DIGITAL LOGIC
(ECEN 2104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The data format used to store data in a digital computer is
(a) Octal (b) BCD
(c) Decimal (d) Hexadecimal.

(ii) Minterm corresponding to decimal number 15 is
(a) ABCD (b) A'B'C'D' (c) A+B+C+D (d) A'+B'+C'+D'.

(iii) A Flip Flop is a /an
(a) monostable circuit (b) bistable circuit
(c) astable Circuit (d) none of these.

(iv) A combinational circuit
(a) never contains memory element
(b) always contains memory element
(c) may sometimes contain memory element
(d) contains only memory element.

(v) MUX can be used as
(a) Flip flop (b) Counter
(c) Logic element (d) 7 segment LED driver.

(vi) An n-bit parallel adder consists of
(a) (n+1) full-adders (b) (n-1) full-adders
(c) n full-adders (d) 2n full-adders.

(vii) Gray Code of $(110101)_2$ is
(a) 101111 (b) 100110 (c) 111010 (d) 101011.

(viii) Race around condition is avoided using
(a) J-K flip flop (b) look ahead carry generator
(c) edge triggered flip flop (d) faster gates.

(ix) Don't care condition is
(a) logic 0 (b) logic 1
(c) logic 0 or Logic 1 where ever required (d) none of the above.

(x) In general, a sequential logic circuit consists of
(a) only flip flops
(b) only gates
(c) flip flops and combinational logic circuits
(d) only combinational logic circuits.

Group – B

2. (a) Determine the canonical sum-of-products representations of the function f(x,y,z) = z + (x' + y) (x + y')

(b) Design a 2-bit magnitude comparator circuit using logic gates.

6 + 6 = 12

3. (a) Simplify the minimal sum of the products for the Boolean expression, $f(A,B,C,D) = \sum m(0,4,5,6,7,8,9,15)$ using the Quine McCluskey method.

(b) Simplify the expression $Y = \sum m(0, 3, 5, 7, 9, 13, 14, 15)$ using K-map method.

8 + 4 = 12

Group – C

4. (a) Design a full-adder circuit using half adders and necessary logic gates.

(b) Implement the function f (a, b, c) $= \sum m$ (1, 3, 5, 6) using a *4:1* line Multiplexer.

6 + 6 = 12

5. (a) Implement the following function using a 3 to 8 decoder:
S (A,B,C) = $\sum$ m(1,2,4,7)
C (A,B,C) = $\sum$ m (3,5,6,7)

(b) Implement the function f (a,b,c) = $\sum m$ (0,1,4,6) using a 1-to-8 Demultiplexer.

8 + 4 = 12

Group – D

6. (a) Develop the characteristic equation of J-K flip-flop from the present state next state table.

(b) Realize a J-K flip flop using S-R flip flop.

(c) What is race around condition?

4 + 6 + 2 = 12

7. (a) Realize D flip-flop using T flip-flop.

(b) Design and implement a MOD 3 synchronous counter using J-K flip-flop.

6 + 6 = 12

Group – E

8. Write a short note on:

(i) Analog to Digital converter using Successive Approximation Register (SAR).
(ii) Digital to Analog converter using R-2R ladder.

6 + 6 = 12

9. Write a short note on (any two): **(6 × 2) = 12**
(i) PLA
(ii) CMOS NAND gate
(iii) ROM.