SPECIAL SUPPLE B.TECH/AEIE/IT/7TH SEM/ECEN 4181/2018

VLSI DESIGN AUTOMATION
(ECEN 4181)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) VLSI technology uses _____ to form integrated circuit.
(a) transistors (b) switches
(c) diodes (d) buffers.

(ii) Medium scale integration has
(a) ten logic gates (b) fifty logic gates
(c) hundred logic gates (d) thousands logic gates.

(iii) The design flow of VLSI system is
1. Architecture design 2. Market requirement
3. Logic design 4. HDL coding
(a) 2-1-3-4 (b) 4-1-3-2
(c) 3-2-1-4 (d) 1-2-3-4.

(iv) Which provides higher integration density?
(a) Switch transistor logic (b) Transistor buffer logic
(c) Transistor transistor logic (d) Circuit level logic.

(v) Which is the high level representation of VLSI design?
(a) Problem statement (b) Logic design
(c) HDL program (d) Functional design.

(vi) In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging and discharging of load capacitance?
(a) Static dissipation (b) Dynamic dissipation
(c) Both (a) and (b) (d) None of the above.

(vii) In accordance to the scaling technology, the total delay of the logic circuit depends on _____?
(a) the capacitor to be charged
(b) the voltage through which capacitance must be charged
(c) available current
(d) all of the above.

(viii) _____ is the fundamental architecture block or element of a target PLD.
(a) System partitioning (b) Pre-layout simulation
(c) Logic cell (d) Post-layout simulation.

(ix) Which among the following operation/s is/are executed in physical design or layout synthesis stage?
(a) Placement of logic functions in optimized circuit in target chip
(b) Interconnection of components in the chip
(c) Both (a) and (b)
(d) None of the above.

(x) Which type of MOSFET exhibits no current at zero gate voltage?
(a) Depletion MOSFET (b) Enhancement MOSFET
(c) Both (a) and (b) (d) None of the above.

Group – B

2. (a) Why low power has become an important issue in the present day VLSI circuit realization?

(b) Briefly describe the voltage transfer curve of CMOS inverter.

(c) How MOS transistor can be used for the purpose of digital switch?

3 + 5 + 4 = 12

3. (a) Draw the stick diagram using Euler path of the expression;
F = A(D+E)+BC ! (! Means bar)

(b) Explain the modes of operations of MOS transistors in depletion mode.

10 + 2 = 12

Group – C

4. (a) State the difference between full custom design and semi-custom design.

(b) Elaborate the VLSI design domain by proper representation of its domain and levels.

5 + 7 = 12

5. (a) Draw the VLSI design cycle showing its front end design and back end design also.

(b) Explain FPGA LUT with the help of a suitable example.

6 + 6 = 12

Group – D

6. (a) With the help of proper block diagram explain the high level synthesis flow steps.

(b) What is the input, output and the basic objective of scheduling?

7 + 5 = 12

7. (a) Write verilog program for 3 to 8 decoder using always and case statements.

(b) Write verilog code for MUX 4:1 in dataflow style and behavioural style.

6 + 6 = 12

Group – E

8. (a) Explain floor planning with fixed and flexible blocks stating its input, output and its objectives?

(b) With the help of a suitable example, explain Maze Routing algorithm.

5 + 7 = 12

9. Write short notes on:
(i) OBDD
(ii) KL algorithm
(iii) Global vs Detailed routing.

4 + 4 + 4 = 12