COMPUTER ORGANIZATION AND ARCHITECTURE
(MCAP 1205)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) What characteristic of RAM memory makes it not suitable for permanent storage?
(a) too slow (b) unreliable
(c) it is volatile (d) too bulky.

(ii) To reduce the memory access time we generally make use of _____
(a) heaps (b) high capacity RAM
(c) SDRAM (d) cache.

(iii) The time delay between two successive initiation of memory operation is
(a) memory access time (b) memory search time
(c) memory cycle time (d) instruction delay.

(iv) In IEEE-32 bit representation mantissa consists of _____ bits.
(a) 24 (b) 23
(c) 20 (d) 16.

(v) The communication between the components in a microcomputer takes place via the address and
(a) I/O bus (b) data bus
(c) address bus (d) control lines.

(vi) Cache memory works on the principle of
(a) locality of data (b) locality of memory
(c) locality of reference and memory (d) locality of reference.

(vii) In case of zero-address instruction method the operands are stored in _____
(a) registers (b) accumulators
(c) push down stack (d) cache.

(viii) The addressing mode where we directly specify the operand value is ____
(a) immediate (b) direct
(c) definite (d) delative.

(ix) When a subroutine is called, the address of the instruction following the CALL instructions is stored in/on the
(a) stack pointer (b) accumulator
(c) program counter (d) stack.

(x) Memory address refers to the successive memory words and the machine is called as _____
(a) word addressable (b) byte addressable
(c) bit addressable (d) tera byte addressable.

Group - B

2. (a) What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer.

(b) Mention the functions of the following processor registers
(i) IR (ii) MAR (iii) PC.

(c) What is the difference between direct and indirect address instruction?

(1 + 5) + (1 + 1 + 1) + 3 = 12

3. (a) Differentiate Von-Neumann architecture and Harvard Architecture. What do you mean by the addressing - mode of an instruction? "Register addressing mode is advantageous rather than using register indirect addressing mode " Justify .

(b) Name the different types of instruction-format with suitable example.

(2 + 2 + 3) + 5 = 12

Group - C

4. (a) Multiply the numbers $(7)_{10}$ and $(-13)_{10}$ using binary 2's complement sign magnitude representation applying Booth's Multiplication algorithm. Draw the hardware structure for implementing Booth's multiplication algorithm.

(b) Find the quotient and remainder applying binary division restoring algorithm where dividend=$(10)_{10}$ and divisor=$(3)_{10}$. Draw the hardware structure for the above method.

(5 + 2) + 5 = 12

5. (a) What do you mean by fixed point representation? Explain the various integer representations with suitable example.

(b) Express $(13.625)_{10}$ in IEEE-754 32 bit representation.

(2 + 5) + 5 = 12

Group - D

6. (a) Draw the memory hierarchy regarding size, speed, cost per bit. Briefly explain different types of locality of reference.

(b) What is write-through and write-back protocol? Which one is more simpler than other ? Justify your answer .

(3 + 4) + 5 = 12

7. (a) Consider a Cache consisting of 128 blocks of 16 words each. Assume that main memory has 4K blocks of 16 wards each. Discuss the advantage or disadvantages of associative mapping over direct memory-mapping for these memory sizes if we assume that main memory is addressable by 16-bit address.

(b) Write short notes on the following
(i) Daisy-chaining technique. (ii) Address translation mechanism in virtual memory.

5 + 3 + 4 = 12

Group - E

8. (a) What is input-output interface? Draw and explain block diagram of input-output interface.

(b) What are different pipelining hazards and how are they eliminated?

(4 + 2) + 6 = 12

9. (a) What is the difference between isolated I/O and memory mapped I/O ? Explain arithmetic pipeline with suitable diagram.

(b) Write a short note
(i) Strobe Control method for data transfer
(ii) Handshaking method for data transfer.

(3 + 3) + (3 + 3) = 12