M.TECH/VLSI/2ND SEM/VLSI 5202/2019
VLSI DESIGN, TESTING AND VERIFICATION
(VLSI 5202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The output of physical design is
(a) Layout (b) Mask (c) RTL (d) Circuit Design.

(ii) Below memory can hold the bit value when there is no power supply
(a) DRAM (b) ROM (c) SRAM (d) Register File.

(iii) Data refresh operation is needed in
(a) DRAM (b) EROM (c) EEPROM (d) SRAM.

(iv) In the VTC curve of an inverter critical voltages are obtained, where the shape of the curve (dV_{out}/dV_{in}) is
(a) +1 (b) -1 (c) 0 (d) 0.25.

(v) Wire RC model acts as
(a) High pass filter (b) Low pass filter
(c) Band pass filter (d) All pass filter.

(vi) Transistor performs slowest at
(a) High Voltage, High Temperature
(b) High Voltage, Low Temperature
(c) Low Voltage, High Temperature
(d) Low Voltage, Low Temperature.

(vii) ATPG is based on
(a) Stuck at fault (b) BIST
(c) Bridging fault (d) DFT.

(viii) Signature analyser (SA) is part of
(a) scan design (b) boundary scan
(c) BIST (d) ad hoc DFT.

(ix) Synthesis translates descriptions from
(a) Physical to Behavioural (b) Structural to Physical
(c) Behavioural to Structural (d) Structural to Behavioural.

(x) VHDL is a
(a) Multi-threaded program (b) C like programming language
(c) Single user program (d) Sequential program.

Group – B

2. (a) Explain briefly with schematic the operation of a CMOS inverter.

(b) Design a one bit Full Adder, showing the transistor level schematic circuit and also the gate level schematic.

6 + 6 = 12

3. (a) Explain write "0" into a SRAM cell with proper circuit diagram and timing waveforms.

(b) Explain read "0" from a SRAM cell with proper circuit diagram and timing waveforms.

6 + 6 = 12

Group – C

4. (a) Explain differences between differential Pair Sense Amplifier vs Latch based Sense Amplifier with circuit diagram.

(b) What is best circuit scheme to create 8 to 256 bit decoder, explain with diagram.

6 + 6 = 12

5. (a) As per process technology, Metal-6 resistance is 100 mohms/μm and capacitance is 0.2fF/μm. If 1mm wire is routed using Metal-6, draw circuit diagram of 3 segment pi model with appropriate resistance and capacitance values of individual segments.

(b) Why driver side of a wire needs to have low resistance and receiver side of the wire needs to have low capacitance, explain using Elmore delay model.

6 + 6 = 12

Group – D

6. (a) For a flip flop based sequential circuit, Cycle Time = 300 ps, Setup Time = 20 ps, Clock-Skew = 30 ps, Combinational Delay = 80ps, Clock to Out Delay of Flop = 40 ps. Hold Time = 50 ps. What is setup margin and hold margin for the Circuit ?

(b) What is clock skew and what are sources of Clock Skew ?

6 + 6 = 12

7. (a) Explain H-Tree of clock distribution using circuit diagram

(b) Design a two input multiplexer gate using two CMOS transmission gate switches.

6 + 6 = 12

Group – E

8. (a) Find the reject rate in PPM for a PCB with 50 chips, where each chip has 80% fault coverage and 80% yield. What happens to the defect level if fault coverage per chip is improved to 90% ?

(b) Explain with example the effect of gate delay fault in a combinational circuit?

8 + 4 = 12

9. (a) Explain how Level Sensitive Scan Design Flip Flop (LSSD-SFF) works using circuit diagram.

(b) Explain Scan Design Methodology with flow diagram.

6 + 6 = 12