Group - D

6. (a) Explain DNL and INL in analog-to-digital converters. Is any ADC possessing a DNL is guaranteed to have a Missing Code? Justify your answer.

   (b) Explain the operation of a Flash ADC. Briefly discuss its accuracy issues.

(4 + 2) + (4 + 2) = 12

7. (a) Explain the operation of DAC architecture with R-2R ladder network.

   (b) Discuss the role of "Dummy Switch" in this architecture.

   (c) Design a 3-bit DAC using an R-2R architecture with R=1kΩ, R_f=2 kΩ and V_{REF}=5V. Assume that the resistances of the switches are negligible. Determine the value of i_{tot} for each digital input and the corresponding output voltage V_{out}.

4 + 2 + 6 = 12

Group - E

8. (a) Emulate the Resistor equivalent of a Parallel Switched capacitor circuit.

   (b) Using Switched capacitor techniques, implement the circuit shown in the Fig. 2, so that the product of RC is 1mS, that is, the 3-dB frequency of $|V_{out}/V_{in}|$ is 159Hz.

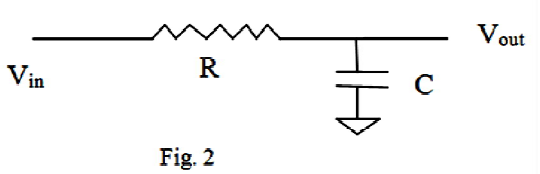

Fig. 2

6 + 6 = 12

9. (a) Explain the operation of three stage ring oscillator.

   (b) Analyse what happens if in the three stage ring $A_0 \neq 2$.

   (c) Determine the maximum voltage swing of each stage of a three stage ring oscillator incorporating differential pair with resistive loads.

5 + 4 + 3 = 12

ANALOG VLSI IC DESIGN
(VLSI 5201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

   (i) MOS device being symmetric
   (a) doping concentration of source terminal should be higher compared to drain terminal
   (b) source and drain terminals are interchangeable
   (c) doping concentration of source terminal should be lesser compared to drain terminal
   (d) source and drain terminals are not interchangeable.

   (ii) The number of stages in a ring oscillator is determined by various requirements including
   (a) speed (b) power dissipation
   (c) noise immunity (d) all of the above.

   (iii) In order to realize MOS device as a zero-offset switch, it should be operated in
   (a) deep triode region (b) triode region
   (c) either linear or saturation region (d) saturation region.

   (iv) The frequency of the signal applied to the switched-capacitor circuit should satisfy the criteria
   (a) $f_{signal} << f_{clock}$ (b) $f_{signal} >> f_{clock}$
   (c) $f_{signal} = 2\, f_{clock}$ (d) $f_{clock} = 2\, f_{signal}$.

   (v) The ENOB of a DAC is defined as
   (a) $(SNR_{actual} - 1.76)/6.02$ (b) $(SNR_{max} - 1.76)/6.02$
   (c) $(SNR_{actual} + 1.76)/6.02$ (d) $(SNR_{max} + 1.76)/6.02$.

(vi) The folded – cascode op-amp has
(a) higher power dissipation and higher voltage gain than telescopic configuration
(b) lower power dissipation and higher voltage gain than telescopic configuration
(c) lower power dissipation and lower voltage gain than telescopic configuration
(d) higher power dissipation and lower voltage gain than telescopic configuration.

(vii) The primary disadvantages of the switched capacitor circuits are
(a) necessity of the bandwidth of the signal being less than the clock frequency
(b) necessity of the bandwidth of the signal being greater than the clock frequency
(c) requirement of non – overlapping clock
(d) both (a) & (c).

(viii) Considering V_{REF} = 1V, as the digital word increases by 1 bit, the output of the ideal 3-bit DAC should jump by
(a) 0.25V (b) 0.0625V (c) 0.33V (d) 0.125V.

(ix) Practical current mirror circuits deviate from ideal behaviour due to
(a) channel length modulation effect
(b) threshold voltage offset between two transistors
(c) imperfect geometrical matching
(d) all of the above.

(x) An ideal differential amplifier should have CMRR
(a) 0 < CMRR < 1 (b) one (c) infinite (d) zero.

Group - B

2. (a) Draw and explain the high-frequency small-signal equivalent circuit of the MOSFET.

(b) Mention the advantages of differential operation over single-ended operation.

(c) Calculate the differential gain of a basic resistive load differential amplifier circuit.

5 + 2 + 5 = 12

3. (a) Briefly discuss the limitations of the MOS switch and also the methods adopted to reduce them.

(b)

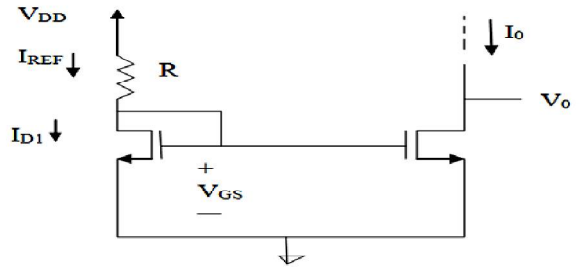

Fig. 1

In the circuit shown in Fig. 1 given V_{dd}=3V and using I_{REF}=100μA, it is required to design the above circuit to obtain an output current whose nominal value is 100μA. Find R if both the MOS are matched and have channel lengths of 1μm, channel widths of 10μm, V_t=0.7V and k_n'=200μA/V². What is the lowest possible value of V_0? Assuming that for this process technology the Early voltage V_A'=20V/μm, find the output resistance of the current source. Also find the change in output current resulting from a +1V change in V_0.

6 + 6 = 12

Group - C

4. (a) Distinguish between the time variance and non-linearity attribute of an RF circuit.

(b) A 900 MHz GSM transmitter delivers a power of 1watt to the antenna. By how much must the second harmonic of the signal be suppressed (filtered) so that it does not desensitize a 1.8GHz receiver having P_{1db}=−25 dBm? Assure that the receiver is 1m away and the 1.8GHz signal is attenuated by 10dB as it propagates across the distance.

(c) Discuss briefly the phenomenon of Cross Modulation. Suppose an interferer contains phase modulation but not amplitude modulation, does Cross Modulation occur in this case?

4 + 4 + 4 = 12

5. (a) Explain Skin Effect. Does "Current Crowding" effect influence inductance and capacitance of Spiral Geometries? Justify your answer.

(b) Estimate the power lost in the substrate using a distributed model of a spiral inductor.

(3 + 4) + 5 = 12