DIGITAL VLSI DESIGN
(ECEN 3201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) VLSI technology uses _____ to form integrated circuit
(a) transistors (b) switches
(c) diodes (d) buffers

(ii) In Pseudo-nMOS logic, n transistor operates in
(a) cut off region (b) saturation region
(c) resistive region (d) linear region.

(iii) According to Moore's Law, Number of Transistor per chip gets doubled in
(a) 12 Months (b) 18 Months
(c) 24 Months (d) 30 Months.

(iv) Latest Integration Technology is
(a) LSI (b) VLSI
(c) ULSI (d) GSI.

(v) The noise immunity _____ with noise margin
(a) increases (b) decreases
(c) remains constant (d) remains independent

(vi) Stick diagrams are those which convey layer information through
(a) thickness (b) colours
(c) layers (d) shapes.

(vii) Value of "Lambda" in 130nm Process Node is
(a) 130nm (b) 65nm
(c) 180nm (d) 100nm.

(viii) BDD is used in
(a) High Level Synthesis (b) Logic Synthesis
(c) Floorplan (d) Routing.

(ix) KL Algorithm is related to
(a) Routing (b) Partitioning
(c) Logic synthesis (d) High level synthesis.

(x) ATPG stands for
(a) Advanced Test Pattern Generator
(b) Active Test Pattern Generator
(c) Automatic Test Pattern Generator
(d) Both b and c.

Group - B

2. (a) What are the differences between Full Custom Design and Std Cell based Semi Custom Design ?

(b) Draw Circuit Diagram of 2 input XOR gate using CMOS Logic.

(c) Draw Circuit Diagram of 2 input XOR gate using CMOS Transmission Gate (TG).

4 + 4 + 4 = 12

3. (a) Draw Voltage Transfer Characteristic curves of a CMOS inverter for k_r = 0.5, 1 and 3 in the same graph. Briefly explain the differences in the three curves.

(b) Draw the CMOS circuit of the expression Y=$\overline{\{A(B+C)\}+D}$. Calculate the logical effort for all the inputs.

(c) Implement a 4- input AND gate using Domino logic.

(2 + 2) + 4 + 4= 12

Group - C

4. (a) Draw Circuit Diagram of a D-Latch using CMOS Transmission Gate (TG).

(b) Draw Circuit Diagram of a Positive Edge Triggered D-Flip Flop using D-Latch.

(c) Explain Euler Path solution of a CMOS gate which represents function f = (AB+C) ! (! Means Bar) and draw Stick Diagram of the same CMOS gate based on Euler Path Solution.

3 + 3 + (3 + 3) = 12

5. (a) Draw Layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

(b) What is the difference between “Micron based Design Rule” and “Lambda Based Design Rule” ?

(c) Draw schematic and Stick Diagram of 2 input NAND gate.

4 + 3 + 5 = 12

Group - D

6. (a) What do you mean by Bit Swizzling? State with example the types of circuit modelling using HDL.

(b) Write an HDL module for a 2:4 decoder.

(c) Discuss the limitations of RTL synthesis.

(2 + 4) + 4 + 2 = 12

7. (a) Write the verilog code for a 4-bit counter.

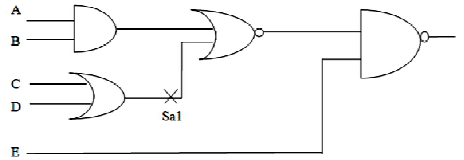
(b) Write a verilog program for a Moore machine.

(c) What is compaction?

4 + 6 + 2 = 12

Group - E

8. (a) Find the test vector of the following circuit using D-algorithm. Write the logic statements clearly.



(b) What do you understand by transistor fault? Write the truth –table for the fault-free and faulty Nor gate considering all the MOS-components are at stuck on and stuck off fault one at a time.

(c) What is path delay fault?

5 + 5 + 2 = 12

9. (a) Discuss the different types of bridging faults with the help of necessary diagrams.

(b) Design the block diagram of a test generator for a 4K×32 static RAM.

6 + 6 = 12