DIGITAL ELECTRONICS
(ECEN 2002)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which one of the following is a weighted code?
(a) 2421 (b) Excess-3
(c) Gray (d) None of these.

(ii) The code used for labelling cells of the K-map is
(a) natural BCD (b) Hexadecimal
(c) Gray (d) Octal.

(iii) The terms which cannot be combined further in the tabular method are called
(a) redundant prime implicants (b) prime implicants
(c) essential prime implicants (d) implicants.

(iv) The 2's complement representation of $(-19)_{10}$ is
(a) 101100 (b) 101110
(c) 101101 (d) none of these.

(v) In which of the following adder circuits is the carry ripple delay eliminated?
(a) Carry-look ahead adder (b) Full-adder
(c) Parallel-adder (d) Half-adder

(vi) If $(212)_x = (23)_{10}$, then the value of x is
(a) 2 (b) 3 (c) 4 (d) 5.

(vii) Master-slave configuration is used in flip-flop to
(a) increase its clocking rate (b) reduce power dissipation
(c) eliminate race-around condition (d) improve its reliability.

(viii) To add two m-bit numbers, the number of required half adder is
(a) 2m-1 (b) 2m (c) 2^m (d) 2m+1.

(ix) The number of flip-flops required for a mod-16 ring counter is
(a) 4 (b) 8 (c) 15 (d) 16.

(x) In general, a sequential logic circuit consists of
(a) only flip-flops
(b) only gates
(c) flip-flops and combinational logic circuits
(d) only combinational logic circuits.

Group - B

2. (a) Simplify the Boolean function using K-map
$f(A, B, C, D) = \sum m(0,1,4,5,9,11,14,15) + \sum d(10,13)$.

(b) Subtract (-9) from (+12) in 2's complement system

7 + 5 = 12

3. (a) Simplify the following function using tabular method
$f(A, B, C, D) = \sum m(0,4,7,9,13,15) + \sum d(10,14)$.

(b) Write the decimal equivalent codes for the flowing canonical POS function
$f(X, Y, Z) = (X + Y + \bar{Z})(X + \bar{Y} + \bar{Z})(X + Y + Z)(\bar{X} + Y + \bar{Z})(\bar{X} + \bar{Y} + \bar{Z})$.

(c) Perform the following conversion
(i) $(1011011110100101.001111)_2$ to HEX
(ii) $(1001010011.10010101)_2$ to Octal.

6 + 3 + 3 = 12

Group - C

4. (a) Design a 16:1 multiplexer using 8:1 multiplexers and necessary logic gates.

(b) What are the difference between Decoder and Demultiplexer?

(c) Design a 4-to-16 Decoder from Two 3-to-8 Decoders.

5 + 3 + 4 = 12

5. (a) Use a 4X1 Multiplexer to implement the logic function
F(A, B, C) =$\sum m(1, 2, 4, 7)$

(b) Realize a half-Adder using only NAND gates.

(c) What are RAM and ROM?

5 + 4 + 3 = 12

Group - D

6. (a) Design a JK flip-flop using S-R flip-flop.

(b) What is the difference between a latch and an edge triggered flip-flop?

(c) Explain the working principle of SERIAL-IN, PARALLEL-OUT shift register with suitable logic diagram.

5 + 3 + 4 = 12

7. (a) Design a decade counter using J-K flip-flop.

(b) Draw the circuit diagram of a bidirectional shift register using D flip-flop and explain the same.

6 + 6 = 12

Group - E

8. (a) Draw a neat diagram of an R-2R ladder type DAC and explain its operation.

(b) Describe the basic principle of Successive Approximation Method for A/D Converter.

(c) Define the following parameters of DACs
(i) Resolution (ii) Step Size.

5 + 5 + 2 = 12

9. Write short notes on any *three* of the followings:
(i) Flash-type ADC
(ii) EEROM
(iii) CMOS
(iv) Tri-state gates in TTL family
(v) Single bit comparator.

4 + 4 + 4 = 12