B.TECH/CSE/8TH SEM/ECEN 4283/2019
VLSI TESTING AND VERIFICATION
(ECEN 4283)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) For Sub Micron Technology L_{gate} (Channel Length) is
(a) >100 nm (b) < 100 nm (c) >1μm (d) None of these.

(ii) Output of physical design is
(a) circuit (b) layout (c) logical model (d) RTL schematic.

(iii) In PVT analysis the variational sources considered are ___, ___, and temperature.
(a) pressure, volume (b) progress, value
(c) process, voltage (d) performance, volume.

(iv) A MOS device can be used as a resistor in
(a) linear Region (b) saturation region
(c) sub-threshold condition (d) mask region.

(v) ATPG is based on
(a) stuck at fault (b) BIST (c) bridging fault (d) DFT.

(vi) As per Moore's Law, area of transistor is scaled by
(a) 0.5 (b) 0.6 (c) 0.9 (d) 0.7.

(vii) A short between two elements is referred to as
(a) timing fault (b) bridging fault (c) series fault (d) decision fault.

(viii) The noise immunity of the circuit _____ with noise margin.
(a) increases (b) decreases (c) is constant (d) zeros.

(ix) CMOS stands for _____ Metal Oxide Semiconductor
(a) Complementory (b) Common (c) Curious (d)Controlled.

(x) Stick diagram helps
(a) logic design (b) circuit design
(c) layout design (d) architecture design.

Group – B

2. (a) Explain with schematic the operation of a CMOS inverter. Describe its VTC characteristics. What are its advantages over other MOS inverters?

(b) Design a CMOS based 2 input NOR gate, explaining operation of the pMOS and nMOS network.

7 + 5 = 12

3. (a) Implement 2 input AND gate using Pass Transistor Logic.

(b) Implement 2 input XOR gate using Transmission Gate (TG) Logic.

6 + 6 = 12

Group – C

4. (a) Sketch the Y chart for simplified VLSI design flow in three domains.

(b) In VLSI, what are full–custom and semi–custom designs and design with FPGA?

(c) In VLSI design, explain the concepts of regularity, modularity, and locality.

4+ 4 + 4 = 12

5. (a) What is Moore's law?

(b) Draw cross sectional diagram of a CMOS Inverter.

(c) Draw schematic diagram of a 3-input NAND Gate.

(d) Draw stick diagram of same 3-input NAND gate.

2+ 3 + 2 + 5 = 12

Group – D

6. (a) What are DRC and LVS?

(b) Why do we need post layout timing verification?

(c) Define setup time and hold time of a D-Latch.

(d) What is process variation?

3+ 3 + 3 + 3 = 12

7. (a) Explain the effects of gate delay fault? What is the critical path in a circuit? What is meant by the capture path?

(b) What is clock skew and what are the sources of clock skew?

8 + 4 = 12

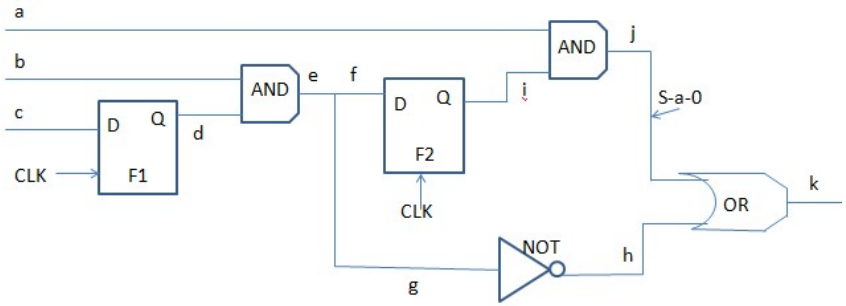
Group – E

8. (a) Why is post Si debugging needed ?

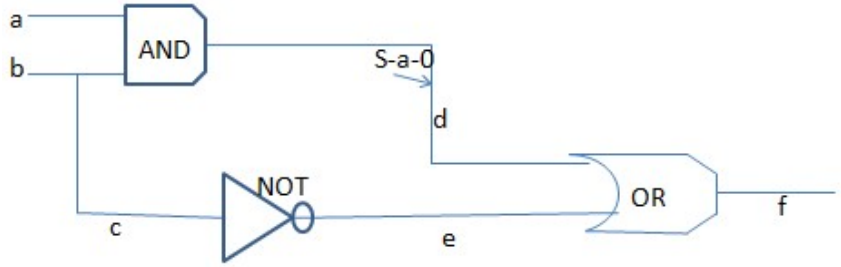
(b) Explain D-Algorithm with an example circuit.

6 + 6 = 12

9. (a) Using ATPG time frame expansion method, generate primary input test patterns for the S-a-0 fault, at the line j in the sequential circuit given below.



(b) Using ATPG path sensitization, generate primary input test patterns for the S-a-0 fault, at line d in the combinational circuit given below.



8+4 = 12