B.TECH/CSE/4TH SEM/CSEN 2203/2019
COMPUTER ORGANIZATION
(CSEN 2203)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) How many address lines are needed to address each memory location in 2046 × 8 memory chip?
(a) 8 (b) 10 (c) 11 (d) 12.

(ii) The CPU is bypassed and the data are directly transferred from external device to the system memory in ……..
(a) programmed I/O (b) interrupt driven I/O
(c) DMA (d) non-programmed I/O.

(iii) The principle of locality justifies the use of
(a) interrupt (b) DMA (c) cache memory (d) polling.

(iv) Which of the following are true for n-bit signed number representation?
1. The minimum and maximum number that can be represented in sign magnitude is $-(2^{n-1}-1)$ and $+(2^{n-1}-1)$
2. The minimum and maximum number that can be represented in one's complement is -2^{n-1} and $+(2^{n-1}-1)$
3. The minimum and maximum number that can be represented in two's complement is -2^{n-1} and $+(2^{n-1}-1)$

(a) both 1 and 2 (b) both 2 and 3 (c) both 1 and 3 (d) all 1 ,2 and 3.

(v) The access time of memory is ……. the time required for performing any single CPU operation:
(a) shorter than
(b) negligible than
(c) same as
(d) longer than.

(vi) Address for the next executable instruction is stored in the
(a) stack pointer (b) program counter
(c) instruction register (d) none of these.

(vii) A stack organized computer uses
(a) indirect addressing (b) index addressing
(c) zero addressing (d) two addressing .

(viii) The performance of cache memory is frequently measured in terms of a quantity called
(a) hit ratio (b) miss ratio (c) latency ratio (d) read ratio .

(ix) Which of the following is not the cause of possible data hazards?
(a) RAR (b) RAW (c) WAR (d) WAW.

(x) A 4 way set associative cache memory unit with a capacity of 16 KB is built using block size of 8 words. The word length is 32 bits. The size of the physical address space is 4GB. The no of bits for TAG field is
(a) 15 (b) 20 (c) 23 (d)25

Group – B

2. (a) What is addressing mode? Briefly explain different types of addressing modes. Registers R1 and R2 contain data values 1800 and 3800 respectively in decimal, and the word length of the processor is 4 bytes.

(b) What will be the effective address of the memory operand for the instruction "ADD 100(R2),R6" ?

(c) Registers R1 and R2 contain data values 600 and 800 respectively in decimal, and the word length of the processor is 4 bytes. What will be the effective address of the memory operand for the instruction "LOAD R5,10(R1,R2)" ?

8 + 2 + 2= 12

3. (a) What are the different types of instruction formats? Explain briefly with examples.

(b) There are 50 registers, and total 55 instructions available in a general purpose computer. The computer allows only 2-address instructions, where one operand can be a register and another can be a memory location. The memory is byte addressable with 64KB (Kilo Bytes) in size. What will be the minimum number of bits to encode the instruction? Give details of instruction format.

8 + 4 = 12

Group – C

4. (a) Represent the following floating point numbers using IEEE (single precision) format:
(i) -0.75
(ii) 2.15

(b) Perform each step of the restoring division algorithm using binary with dividend 8 and divisor 3.

(c) What is the largest possible value for an n-bit 2's complement binary number?

5 + 6 + 1 = 12

5. (a) Discuss the principle of carry look ahead adder. Design a 4 bit CLA. What are the advantages and disadvantages of CLA over RCA.

(b) What are the gate delays for a 4-bit RCA?

(4+ 4 + 2) + 2 = 12

Group – D

6. (a) What is delayed branching?

(b) Consider a 4-segment pipeline with 10 ns clock period. Find out the speedup for 200 tasks.

(c) Explain the concept of a structural hazard in pipelines (using diagram).

(d) Differentiate between RAW and WAR dependencies with examples.

4 + 3 + 3 + 2 = 12

7. (a) What are the advantages of micro-programmed control over hardwired control?

(b) Specify the different types of control signals generated in each stage for the execution of the instruction Move(R1),R2.

(c) Draw the block diagram of control memory (4096 words of 24 bits each) and the associated hardware for selecting the next microinstruction address.
(i) How many bits are there in the control address register?
(ii) How many bits are there in each of the four inputs of multiplexer?

3 +3 + 6 = 12

Group – E

8. (a) What is an interrupt? What are the differences between vectored and non vectored interrupts?

(b) Explain the concept of DMA transfer with a diagram and detailed description.

(2 + 4) + 6 = 12

9. (a) Consider a 4-way set associative cache with 128 blocks and a block size of 16 bytes. Find out cache block number which will contain the main memory address 1200.

(b) A hierarchical Cache-MS memory has the following specifications:
- Cache access time of 90 ns;
- Main memory access time of 500 ns;
- 80% of memory references are for read and 20% for writes;
- Hit ratio of 0.9 for read accesses and 0.80 for write access;
- Probability of setting flag bit is 0.5;

(i) Compute average access time for read (considering both write through and write back).
(ii) Compute average access times for both read and write (considering both write through and write back).

5 + 7= 12