DIGITAL ELECTRONIC CIRCUITS
(AEIE 2201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) A 3-bit adder circuit requires _____.
(a) two full adder and two half adders (b) three full adders
(c) two full adder and one half adders (d) one full adder and two half subtractors.

(ii) The logic function $\overline{X}\overline{Y}Z + \overline{X}YZ + X\overline{Y}$ is equivalent to
(a) X + YZ (b) $\overline{X}Z + X\overline{Y}$
(c) $XZ + \overline{Y}$ (d) $\overline{Y} + \overline{X}\overline{Z}$

(iii) Gray equivalent of the binary code 111001 is
(a) 101101 (b) 100110
(c) 101110 (d) 110011.

(iv) A buffer can be realized by a 2- input X-OR gate when
(a) both inputs are at logic 1 (b) one input is at logic 0
(c) one input is at logic 1 (d) both inputs are at logic 0.

(v) A D-flip flop can be realized through using S-R flip flop by
(a) connecting S and R input together
(b) connecting S and R input through an XOR gate
(c) connecting S and R input through an inverter
(d) none of the above.

(vi) Toggle state in a J-K flip-flop occurs at
(a) J = K = 0 (b) J = 1, K = 0
(c) J = 0, K = 1 (d) J = K = 1.

(vii) The terminal count of a typical modulus-15 binary counter is _____
(a) 1000_2 (b) 1110_2 (c) 1111_2 (d) 1101_2.

(viii) How many flip-flops are required to make a mod-9 counter?
(a) 3 (b) 8 (c) 9 (d) 4.

(ix) In PLA design, we need
(a) fixed AND array and programmable OR array
(b) fixed AND and OR array
(c) programmable AND and OR array
(d) programmable AND array and fixed OR array.

(x) The logic circuit having lowest propagation delay is _____.
(a) TTL (b) ECL (c) CMOS (d) DTL.

Group – B

2. (a) Design a 4-bit full adder circuit using carry look ahead adder (CLA) logic. Write down the advantage of this circuit over normal adder circuit.

(b) What is the difference between combinational and sequential circuit?
(6 + 3) + 3 = 12

3. (a) Subtract (6-15) using 5-bit signed binary number representation.

(b) Minimize the logic function
Y(A, B, C, D, E) = ∑m(1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, 31) by using Karnaugh map.
4 + 8 = 12

Group – C

4. (a) Design a 4-bit Gray to binary code converter.

(b) Realize an 8:1 multiplexer by using 2:1 multiplexers.
7 + 5 = 12

5. (a) Design a full adder circuit using 4:1 multiplexers.

(b) Design a T- flip flop with truth table by using only NAND gates.
8 + 4 = 12

Group – D

6. (a) Design a modulo-16 synchronous counter and explain with output waveforms.

(b) Design an asynchronous counter to start the count at 3 and stop the count at 7 and start the count again from 3.
6 + 6 = 12

7. (a) Design a ripple counter to start the count at 3 and stop the count at 12 and start the count again from 3.

   (b) Write short note on Ring counter.

8 + 4 = 12

Group – E

8. (a) Implement the given functions using programmable logic array (PLA) X(a,b,c,d) = ∑m(0,2), Y(a,b,c,d) = ∑m(4,6,12,14) and Z(a,b,c,d) = ∑m(4,6,8,10).

   (b) Write short notes on successive approximation type ADC and R-2R Ladder type DAC.

6 + 3 + 3 = 12

9. (a) Implement the following logic functions using PROM.
   A = ∑m(0,2,4,6,8), B = ∑m(1,3,5,7)

   (b) Design a NOR gate using CMOS logic.

7 + 5 = 12