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Influence of Underlap on Gate Stack DG-MOSFET for analytical study of Analog/RF performance

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In this paper, the characteristics of 18 nm Underlap Double Gate (U-DG) NMOSFET with gate stack, (GS) are presented. The high-*k* dielectric as gate insulator under consideration is Hafnium Dioxide (HfO_2). The SiO_2 padding reduces the effect of scattering at the silicon and oxide interface. The ratio of on current to off current is used for optimizing the underlap length. The Analog and RF performance comparison are shown in this paper considering the drain current (I_d), the transconductance (g_m), the intrinsic gain (g_mR_o), the intrinsic capacitances (C_{gs}, C_{gd}), the intrinsic resistances (R_{gs}, R_{gd}), the transport delay (τ_m), the intrinsic inductance (H_{sd}), the unity current gain cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}). RF parameters are extracted using the Non Quasi Static (NQS) model of the U-DG MOSFET. The performance of single stage amplifiers using the devices is also analyzed. The sharpest transition is shown in case of U-DG-GS MOSFET with optimized underlap length and enhancement in the intrinsic capacitances and resistances, and unity Gain Bandwidth product in case of devices with GS.

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1. Introduction

The recent advancements in technology and increasing demands for high speed devices with low power consumption have pushed device dimensions in the nanometer regime. While scaling the channel below 100 nm [1], undesirable phenomena such as Short Channel Effects (SCE) [2] come into effect degrading desired device performance and the gate control over channel. The symmetric underlap double gate (U-DG) NMOSFET is a potential solution to reduce the SCE by controlling the effective channel length $L_{eff} = L_g + 2L_{un}$, where L_g is the gate length, L_{un} is the source/drain underlap length of the device and L_{eff} is the length over which the gate influences the conductivity of the channel [3–7]. The U-DG NMOSFETs structures minimize the Gate Induced Drain Leakage (GIDL) [8] and the fringing capacitance [9]. However, Drain Induced Barrier Lowering (DIBL) is high for small underlap lengths (L_{un}) [10]. Also, the on current (I_{on}) decreases and the channel to source/drain parasitic resistance increases with increase in the underlap length (L_{un}) [3]. Therefore, optimization of the underlap length is required for controlling the SCE and stabilizing the on current (I_{on}) of the device. The optimization of the device is done with respect to on-current to off-current ratio (I_{on}/I_{off}) [10, 11].

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