9. (a) How can the SPICE LEVEL 1 model be developed from the expression of the drain current ?

   (b) Compare the threshold voltage-based, charge-based and surface – potential based compact models for a MOS transistor.

6 + 6 = 12

MODELLING OF VLSI DEVICE (VLSI 5142)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

   (i) Carrier concentration in the biased p-n junction device can be described with the concept of
   (a) Equilibrium Fermi level
   (b) Quasi – Fermi level
   (c) Either Fermi or Quasi – Fermi level
   (d) Maxwell – Boltzman distribution function.

   (ii) If a photon with energy $h\gamma$ is incident on a semiconductor of band gap energy E_g, then the photon will be absorbed if
   (a) $h\gamma = E_g$ (b) $h\gamma < E_g$ (c) $h\gamma > E_g$ (d) $h\gamma \geq E_g$.

   (iii) The drawback of a constant field scaled device in comparison to a constant voltage-scaled device is that
   (a) it is less reliable
   (b) it has more speed and power
   (c) it has less speed and power
   (d) multiple power supplies are required.

   (iv) In a MOSFET, when the current saturates beyond pinch-off, the differential channel resistance becomes
   (a) Low (b) Zero (c) Infinite (d) Very high.

   (v) In an n-channel enhancement type MOSFET, the channel is said to be pinched–off when
   (a) $V_D - V_G = V_T$ (b) $V_G - V_D = V_T$ (c) $V_D - V_G > V_T$ (d) $V_G - V_D < V_T$.

(vi) In the saturation region of operation of the BJT,
(a) Emitter-base junction is forward biased, collector-base junction is forward biased
(b) Emitter-base junction is forward biased, collector-base junction is reverse biased
(c) Emitter-base junction is reverse biased, collector-base junction is reverse biased
(d) Emitter-base junction is reverse biased, collector-base junction is forward biased.

(vii) The collector voltage at which the linearly extrapolated collector current of a BJT reaches zero is known as the
(a) early voltage (b) threshold voltage
(c) cut-off voltage (d) cut-in voltage.

(viii) DIBL can occur if
(a) Source/drain junctions are too deep or the channel doping is too low
(b) Source/drain junctions are too shallow or the channel doping is too low
(c) Source/drain junctions are too shallow or the channel doping is too high
(d) Source/drain junctions are too deep or the channel doping is too high.

(ix) Pao-Sah drain current model considers
(a) drift current transport mechanism
(b) diffusion current transport mechanism
(c) both drift and diffusion current transport mechanism
(d) a novel current transport mechanism.

(x) BSIM3 is an example of
(a) Surface potential based model
(b) Threshold voltage based model
(c) Inversion charge based model
(d) None of these.

Group - B

2. (a) Draw the energy-band diagram, density of states distribution, Fermi-Dirac distribution function and carrier concentration profiles for intrinsic, n-type and p-type semiconductors.

(b) Discuss the effects of temperature and doping on the mobility of carriers in semiconductors.

6 + 6 = 12

3. (a) Illustrate with a suitable schematic, the parasitic resistances in a typical modern n-p-n transistor.

(b) Discuss the effect of the emitter and base series resistances on the collector current.

6 + 6 = 12

M.TECH/VLSI/1ST SEM/VLSI 5142/2018

Group - C

4. (a) Draw the energy band diagram of the MOS structure before and after making the contact with proper labelling.

(b) Explain the capacitance – voltage characteristics of a MOS capacitor for low-frequency operation.

6 + 6 = 12

5. (a) How does the application of substrate bias affect the threshold voltage of a MOSFET?

(b) An n^+ Polysilicon gate nMOS has got $N_a=5\times10^{15}$/cc and the Silicon-dioxide thickness to be 100 Å. If the effective interface charge is 4×10^{10} qC/cm^2, find the oxide capacitance per unit area and the minimum value of the capacitance on the C-V characteristics. Also, determine the threshold voltage of the MOSFET. Given, $n_i= 1.5\times10^{10}$/cc, $\varepsilon_r(Si)=11.8$, $\varphi_{ms}=-0.95V$.

4 + 8 = 12

Group - D

6. (a) What is 'scaling'? What are the different theories of scaling of MOSFETs? Discuss their relative advantages and shortcomings.

(b) Write a short note on ITRS.

(1 + 3 + 4) + 4 = 12

7. (a) Explain the impact of substrate bias and short channel effect on the threshold voltage of the MOSFET.

(b) Briefly discuss the channel length modulation effect.

8 + 4 = 12

Group - E

8. (a) Why are compact MOSFET models required ?Briefly describe the Monte Carlo, Moment Methods and Drift – Diffusion TCAD models for device analysis and design.

(b) Discuss briefly the Physical, Empirical, and Table Look up models for circuit simulation.

(2 + 5) + 5 = 12