VLSI IC FABRICATION
(VLSI 5132)

Time Allotted : 3 hrs   **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and
<u>any 5 (five)</u> from Group B to E, taking <u>at least one</u> from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

    (i)   Quantum device killing defects size are
          (a) Less than 80 Angstrom   (b) Less than 200 Angstrom
          (c) More than 500 Angstrom   (d) none of these.

    (ii) For Industrial epitaxial growth reactors are
          (a) Vertical type   (b) Barrel type
          (c) Horizontal type   (d) none of these.

    (iii) The active components in an Integrated Circuit are
          (a) resistors   (b) capacitors
          (c) transistors   (d) all of the above.

    (iv) Epitaxial Growth of Silicon on Sapphire (SoS) means
          (a) Homoepitaxi   (b) Heteroepitaxi
          (c) Vertical Epitaxi   (d) None of these.

    (v)   Optical masking is used for
          (a) pattern transfer   (b) protection
          (c) cleaning   (d) none of the above.

    (vi) DI water is free from all traces of
          (a) particulate contamination   (b) ionic contamination
          (c) bacterial contamination   (d) all of the above.

    (vii) Interconnections and ohmic contacts are formed in
          (a) ion implantation process   (b) diffusion process
          (c) etching process   (d) metallization process.

(viii) Sputtering is a _____ process
(a) physical　　　　　　　　(b) chemical
(c) mechanical　　　　　　　(d) electrical.

(ix) In shadow printing used in optical lithography, the minimum line width (critical dimension CD) is approximately given by [where λ is the wavelength of exposure radiation and g is the gap between the mask and wafer including the resist thickness]
(a) $\sqrt{\lambda g}$　　　　(b) $\frac{\lambda g}{2}$　　　　(c) λg　　　　(d) $(\lambda g)^{1.5}$.

(x) Which of the following processes is used to form a deep junction?
(a) Ion implantation　　　　(b) Diffusion
(c) Etching　　　　　　　　(d) Oxidation.

Group – B

2. (a) What are the requirements and conditions for the VLSI fabrication lab? Describe in brief.

   (b) Why special clean room garments are necessary for working in VLSI Lab?

   (c) Why Photolithography is preferred to be done in a"Class-10" clean room and in yellow light?

   5 + 3 + 4 = 12

3. (a) Discuss the different types of charges that exist at or near the Si-SiO$_2$ interface of a MOSFET and how these might affect the device performance.

   (b) What is bird's beak?

   10 + 2 = 12

Group – C

4. (a) State the advantages and disadvantages of ion-implantation.

   (b) Use the LSS theory to calculate the implant dose required to give a peak dopant concentration of 5×10^{18} boron atoms cm^{-3} in an n-type Si, doped with 10^{15} phosphorous atoms cm^{-3} when boron is implanted at 200 keV into Si. Given the lateral straggle for boron ions at 200 keV is 0.086 micron.

   7 + 5 = 12

5. (a) A boron doped crystal is measured at its seed end with a four point probe of spacing 1mm. The (v/i) reading is 10 ohms. Consider the solid concentration $C_s=2\times10^{15}$ atoms/cm^3 and the segregation coefficient is 0.8 and the expected reading of fraction of the melt solidified is 0.95. What is the seed end doping?

   (b) Explain the doping profile and the junction depth of diffusion with the help of error function.

   6 + 6 = 12

Group – D

6. (a) State the major constituents of a Photo-resist and explain their function. In Optical lithography, what parameter fundamentally determines the minimum resolvable feature size? Explain your answer briefly.

   (b) Describe with an appropriate diagram an electron-beam lithography system.

   (2 + 5) + 5 = 12

7. (a) What is wet chemical etching? What are the characteristics of an ideal etchant used for wet chemical etching?

   (b) Discuss Buffered Oxide Etching, its advantages and limitations.

   (1 + 5) + 6 =12

Group – E

8. (a) With reference to a CMOS fabrication process:
   State the process steps necessary for the formation of LOCOS structure.

   (b) What is a self aligned gate? How is it formed and what is the necessity of it?

   6 + (2 + 4) = 12

9. (a) List the properties that a material must have to be useful as an interconnect.

   (b) What do you mean by aluminium junction spiking? Discuss how it can be overcome.

   4 + (5 + 3) = 12