DIGITAL VLSI IC DESIGN
(VLSI 5101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Value of "Lambda" in 0.5um Technology is
(a) 0.25um (b) 0.5um (c) 1um (d) 0.125um.

(ii) Pentium 4 chip belongs to below category
(a) VLSI (b) LSI (c) ULSI (d) GSI.

(iii) Most popular interconnect material is
(a) Gold (b) Silver (c) Aluminium (d) Platinum.

(iv) BDD is used in
(a) High Level Synthesis (b) Logic Synthesis
(c) Floorplan (d) Routing.

(v) Minimum Number of Transistors in CMOS logic Y = AB + CD + EF is
(a) 10 (b) 12 (c) 14 (d) 8.

(vi) For a Standard Cell Layout
(a) Width is fixed (b) Height is fixed
(c) Both Height and Width are fixed (d) None of Above.

(vii) KL Algorithm is related to
(a) Routing (b) Partitioning
(c) Logic Synthesis (d) High Level Synthesis.

(viii) Memory Design is normally done using below Method
(a) Full Custom (b) Gate Array
(c) Std Cell based Semi Custom (d) FPGA.

(ix) Most Manual Effort is needed in below VLSI Methodology
(a) FPGA (b) CPLD
(c) Std Cell Based Semi Custom (d) Full Custom.

(x) Stick Diagram Represents
(a) Logic (b) Circuit
(c) Layout (d) Architecture.

Group - B

2. (a) What are various Capacitance Components of a MOS Transistor?

(b) Draw VTC (Voltage Transfer Curve) of CMOS Inverter.

(c) How VTC of CMOS inverter will change if Width of PMOS is increased?

(d) For a CMOS Inverter V_{OH} = 5V, V_{OL} = 0V, V_{IH} = 3.5V, V_{IL} = 2V. What is the Value of NM_H and NM_L?

4 + 3 + 3 + 2 = 12

3. (a) What is the difference between "Micron based Design Rule" and "Lambda Based Design Rule" ?

(b) Draw Layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

(c) Draw schematic of CMOS gate which represents function f = (AB+C) ! (! Means Bar).

(d) Draw Stick Diagram of the same CMOS gate.

2 + 2 + 3 + 5 = 12

Group - C

4. (a) What are differences between Full Custom Design and Std Cell based Semi Custom Design ?

(b) Explain Euler Path solution of a CMOS gate which represents function f = (AB+C+D) ! (! Means Bar).

(c) Draw Y Chart for VLSI Design.

4 + 3 + 5 = 12

5. (a) Solve Euler Path Algorithm for the function f = CD(A + B) ! (! Means Bar).

(b) Draw Stick Diagram accordingly.

(c) Draw Flow Diagram of Front End Design Flow.

4 + 4 + 4 = 12

Group - D

6. (a) Write VHDL code of Behavioural Modelling of a D Flip Flop gate.

(b) Draw Flow Diagram of High Level Synthesis.

(c) Explain ASAP and ALAP Scheduling Algorithm

3 + 4 + 5 = 12

7. Write short notes on below topic
i. FPGA.
ii. Finite State Machine.
iii. Technology Library Mapping for Logic Synthesis.

(3 × 4) = 12

Group - E

8. (a) Create ROBDD Diagram and corresponding optimized Boolean expression.

(b) For below Channel Routing Problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)
Terminal Connection is as follows:
11122563040 ----- Upper Boundary
25055330604 ----- Lower Boundary
0 means no Connection.
Assume HV Layer (V = Metal 1, H = Metal 2).

(c) Provide Optimum Channel Routing Solution for above case using Left Edge Algorithm.

2 + 5 + 5 = 12

9. (a) Draw Flow Diagram of Physical Layout Automation.

(b) For Floor-planning problem, what are inputs, outputs and Objective (Cost) function ?

(c) Explain Lee Algorithm of Maze Routing.

4 + 4 + 4 = 12