M.TECH/CSE/1ST SEM/CSEN 5105 (BACKLOG)/2018
ADVANCED COMPUTER ARCHITECTURE
(CSEN 5105)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Utilization pattern of successive stages of a synchronous pipeline can be specified by
(a) truth table (b) excitation table
(c) reservation table (d) periodic table.

(ii) Which of the following is an example of two-dimensional topologies in static network ?
(a) Mesh (b)$3C^3$ Network (c)Linear Array (d)none of these.

(iii) For two instructions I and J WAR hazard occurs, if
(a) $R(I) \cap D(J) \neq \varnothing$ (b)$R(I) \cap R(J) \neq \varnothing$
(c) $D(I) \cap R(J) \neq \varnothing$ (d)none of these.

(iv) The division of stages of a pipeline into sub-stages is the basis for
(a) pipelining (b) super-pipelining
(c) superscalar (d) VLIW processor.

(v) A 4-ary 3-cube hypercube architecture has
(a) three dimensions with four nodes along each dimension
(b) four dimensions with three nodes along each dimension
(c) both (a) and (b)
(d) none of these.

(vi) Which of the following is true?
(a) RAW,WAR and WAW hazards are possible on any pipeline
(b) WAR and WAW hazards are more natural as these refer to flow dependencies
(c) Use of multiple functional units can reduce the possibility of structural hazards
(d) WAR and WAW hazards can happen even if the pipeline is not a multiple issue.

(vii) The task of vectorizing a compiler is
(a) to find the length of vectors
(b) to convert sequential scalar instructions into vector instructions
(c) to process multi dimensional vectors
(d) to execute vector instructions.

(viii) Array processors perform computations to exploit
(a) temporal parallelism
(b) spatial parallelism
(c) sequential behaviour of programs
(d) modularity of programs.

(ix) A pipeline stage
(a) is sequential circuit
(b) Is combinational circuit
(c) consists of both sequential and combinational circuits
(d) none of these.

(x) What will be the speed up for a 4-segment linear pipeline when the number instructions is 64?
(a) 4.5 (b)3.82 (c)8.16 (d)2.95

Group – B

2. Consider the following reservation table.

	0	1	2	3	4	5
S1	x					x
S2		x			x	
S3			x			
S4				x		
S5		x				x

(i) Determine forbidden latency , permissible latency and initial collision vector.
(ii) Draw the permissible state diagram.
(iii) List all simple cycles. Especially point out the greedy cycles (GC).
(iv) What is minimum average latency (MAL) of the pipeline? Is there any GC corresponding to this MAL?
(v) What is the lower bound on this MAL?

3+ 3+3+ 2+ 1 = 12

3. (a) Assume a 5-stage instruction pipeline. The probability of a branch instruction in an instruction stream is 0.2. There is a 60% chance of a branch being taken. What is the degradation in pipeline performance?
   (b) What are the bounds on MAL?
   (c) Explain operand forwarding technique.
   (d) Explain control hazards and means to avoid these.

3+ 2+ 2+ 5= 12

Group – C

4. (a) Draw the diagram of a 8×8 Omega network built with 2×2 switching elements.
   (b) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node101 simultaneously. Does blocking exist in this case?
   (c) Implement data routing logic of SIMD architecture to compute

$$s(k) = \sum_{i=0}^{k} A_i \text{ for } k = 0, 1, 2.....N-1$$

5 + 2 + 5 = 12

5.(a) Write down matrix multiplication algorithm on SIMD (using n number of PEs).
   (b) Also specify a corresponding time complexity with explanation.
   (c) How can sparse matrix be handled using vector processor?
   (d) What is gather instruction in vector processor?

4 + 3 + 3 +2 = 12

Group – D

6.(a) Draw an ILLIAC IV network (for 16 PEs). How many recalculating stages are required to route a message from PE5 to PE15.

   (b) Show how the following two matrices can be multiplied using a mesh connected network?

$$\begin{bmatrix} 1 & 2 \\ 4 & 5 \end{bmatrix} \quad \begin{bmatrix} 4 & 7 \\ 7 & 6 \end{bmatrix}$$

6 + 6 =12

7. (a) State and explain Amdahl's law.
   (b) How does Amdahl's law and Gustafson's law differ with respect to machine size and problem size?
   (c) Consider the un-pipelined machine with 10ns clock cycles. It uses four cycles for operations and branches whereas five cycles are used for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from pipeline?
   (d) What is locality of reference? Differentiate between temporal and spatial locality.

(2+3) + 2 + 3 + (1+1) = 12

Group – E

8. (a) What is the role played by the concept "token" in a data flow machine?
   (b) Draw data flow graph for the following set of instructions:
   X = A+B
   Y=X/B
   Z=A∗X
   M=Z−Y
   N=Z∗X
   P=M/N
   (c) Explain what problem will occur in the following situation of a multiprocessor machine consisting of two CPUs A and B, each with its own cache:
   (i) A reads from memory location X, then
   (ii) B reads from X, and then
   (iii) A updates the value of X.
   Please state any assumption you have made for analyzing the above situation.

2 +6 + 4 = 12

9. What is cache coherence problem? Suggest methods used to solve cache coherence problem. Compare snooping and directory protocol.

2+5+5= 12