(vii) Voltage follower is a special case of _____.
(a) inverting configuration (b) non-inverting configuration
(c) difference configuration (d) integrator configuration.

(viii) How does the average velocity of charge carriers vary with position along the channel of a modern MOSFET under large drain to source voltage?
(a) The average velocity is constant from the source to the drain.
(b) The average velocity increases from the source to the drain.
(c) The average velocity decreases from the source to the drain.
(d) The average velocity reaches a maximum between the source and the drain.

(ix) PMOS and NMOS circuits are used largely in
(a) MSI functions (b) LSI functions
(c) TTL functions (d) Diode functions

(x) MOSFET input resistance is typically of the order
(a) 10^{10}-$10^{15}\Omega$ (b) 10^{10}-$10^{12}\Omega$
(c) 10^{10}-$10^{21}\Omega$ (d) none

Group – B

2. (a) Perform small signal analysis in a MOS cascade amplifier without the load circuit and derive an expression for voltage gain and output resistance.

(b) Design a MOS cascade amplifier current source to provide a current of 100μA and an output resistance of 500kΩ. Assume the availability of a 0.18μm CMOS technology for which V_{DD}= 1.8V, V_{tp}= -0.5V, μ_pC_{ox}= 90μA/V² and V_A= -5V/μm. Use $|V_{ov}|$= 0.3V and determine L and W/L for each transistor.

7 + 5 = 12

3. (a) Derive an expression for propagation delay in a CMOS inverter with capacitor load. Comment on the relation between propagation delay and capacitance of the load.

(b) Write short note on MOS based active resistor circuit.

(5 + 2) + 5 = 12

Group – C

4. (a) Derive expressions for common mode rejection ratio of 741 op-amp input stage.

(b) Derive expressions for output impedance (R_o)of 741 op-amp.

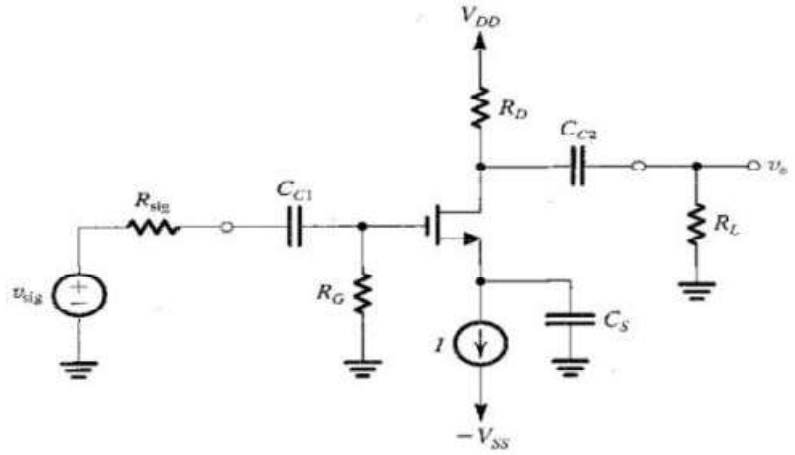
8 + 4 = 12

5. (a) Describe how to convert a monostable multivibrator to an astable multivibrator using suitable circuit diagram.

(b) It is required to connect a transducer having an open-circuit voltage of 1V and source resistance of 1MΩ to a load of 1kΩ resistance. Find the load voltage if the connection is done a) directly and b) through a unity gain voltage follower. **7 + 5 = 12**

Group – D

6. (a) Perform small signal analysis on the given NMOS amplifier circuit, shown in following figure. Find an expression for output impedance and voltage gain.



(b) Compare a bipolar current mirror with MOS mirror. What is bias compensation in a bipolar mirror and how does it improve current transfer ratio?

8 + (2 + 2) = 12

7. (a) Briefly explain the operation of charge-redistribution Analog to Digital Converter.

(b) Obtain the expressions for common mode gain and CMRR for an active loaded MOS differential pair.

6 + 6 = 12

Group – E

8. (a) Consider a CMOS inverter fabricated in a 0.18μm process for which V_{DD}=1.8V, V_{tn}=$|V_{tp}|$ = 0.5V, μ_n=4μp, and μ_nC_{ox}=300μA/V². In addition, Q_N and Q_p have L=0.18μm and $(W/L)_n$=1.5.

(i) Find W_p that results in V_M=V_{DD}/2=0.9V. What is the silicon area utilized by the inverter in this case?
(ii) For the matched case above, find the values of V_{OH}, V_{OL}, V_{IH}, V_{IL} and noise margins NM_L and NM_H. For V_i= V_{IL}, find out the V_o.
(iii) For the matched case above, find the values of output resistance for two inverter output states.

(b) Implement the function $Y = \overline{AB + \overline{A+B}}$ using CMOS realization for AOI gates.

6 + 6 = 12

9. (a) Briefly explain the operation of CMOS transmission gates based switch circuits.

(b) Write short notes on FPGA

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5 + 7 = 12

MICRO-ELECTRONIC DEVICES AND CIRCUITS
(AEIE 5131)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which transistor element is used in CMOS logic?
(a) FET (b) MOSFET (c) Bipolar (d) Unijunction.

(ii) What is the typical input bias current of a 741 operational amplifier?
(a) 70 nA (b) 80 nA (c) 90 nA (d) 100 nA.

(iii) What is the most common method used for growth of single crystals for IC fabrication?
(a) Epitaxial growth (b) Czochralsky pulling technique
(c) Film deposition (d) Photolithography.

(iv) The unity gain frequency of an opamp
(a)Is the frequency where the voltage gain of an opamp is 1
(b) Indicates the highest usable frequency
(c) It equals the gain bandwidth product
(d) All of the above.

(v) The reason why integrated circuits are divided into digital linear categories is because
(a) They either process analog or digital signals
(b) They are either used as input of output components
(c) Up to the present these are the only two known categories
(d) They are simply circuits that happen to be constructed integrally and like all circuits are either switching type or amplifying type.

(vi) What specification of an operational amplifier which tells how fast the output voltage can change?
(a) Frequency response (b) Common mode rejection ratio
(c) Slew rate (d) Open loop voltage gain