# B.TECH/ECE/5TH SEM/ECEN 3104/2018
# MICROPROCESSORS, MICROCONTROLLERS & SYSTEMS
# (ECEN 3104)

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A
## (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) LXI B, 2080H is an example of
(a) 1 - byte instruction (b) 2 - byte instruction
(c) 3 - byte instruction (d) 4 - byte instruction.

(ii) The starting address of 1K Byte memory chip whose last location is FBFFH is
(a) F800 (b) F8FF (c) FB00 (d) F8FE.

(iii) The instruction that should be included in a Service Subroutine to enable the interrupt is
(a)DI (b) EI (c) RESET (d) None of these.

(iv) Which of the following arithmetic or logical instructions will never affect Flag?
(a) INR B (b) ANA B (c) DCX B (d) XRA B.

(v) During ANA instruction, which of the following is true?
(a) Only S and Z flag bits are modified
(b) Only S and P flag bits are modified
(c) S,Z and P flag bits are modified
(d) All the flag bits are modified.

(vi) The instruction which is used to identify the pending interrupts in 8085 is
(a) RIM (b) SIM (c) DAD (d) POP.

(vii) 8259 is
(a) programmable DMA controller
(b) programmable interval timer
(c) programmable interrupt controller
(d) none of these.





(viii) If the crystal with 8085 is 2 MHZ, the time required to execute an instruction of 20 T states is
(a) 20μS (b) 10μS (c) 40μS (d) 5μS.

(ix) The internal RAM memory of the 8051 is:
(a) 32 bytes (b) 64 bytes (c) 128 bytes (d) 256 bytes.

(x) STA 9000H is a
(a) data transfer instruction (b) logical instruction
(c) I/O and machine control instruction (d) None of these.

## Group – B

2. (a) Draw the block diagram of the register section of 8085. Mention the function of Stack Pointer and Program Counter.

(b) Draw the Flag register of 8085.Mention the conditions under which each of the flags goes to Set state.

**(2 + 4) + (2 + 4) = 12**

3. (a) Justify the statement with proper diagram - "Interfacing logic defines the range of memory address for each memory device".

If the memory chip size is 256 × 1bits, how many chips are required to make up 1K byte of memory?

(b) Design an interface on EPROM IC (8K× 8 bits) and two RAM IC (4K × 8 bits and 8K × 8 bits) with the 8085 using 74LS138 address decoder IC such that starting address range allocated to the chip are respectively 0000H, 8000H and A000H.

**(4 + 2) + 6 = 12**

## Group – C

4. (a) Compare CALL and RET and PUSH and POP instructions.

(b) Calculate the total delay in the following program, assuming that the clock frequency of the system is f = 2MHz.

| Label | Opcode | Operand |
|---|---|---|
| | LXI | B,2384H |
| LOOP: | DCX | B |
| | MOV | A,C |
| | ORA | B |
| | JNZ | LOOP |

**5 + 7 =12**

5.(a) Explain the operations of BIU and EU present in 8086 microprocessor.

(b) What is an addressing mode? How many addressing modes are available in 8086? Explain with two examples of each.

**5 + (1 +2 + 4) = 12**

## Group – D

6. (a) Draw the block diagram of 8255A Programmable Peripheral Interface.
What are the unique difference between all the eight lines of port A and port B and port C?

(b) Write the control word format for the I/O mode of 8255A.
Specify the function of Control register.
What is BSR mode?

**4 + 2 + (2+ 2 + 2) = 12**

7.(a) What is the purpose of the operational command words of 8259? Explain the ICW1 format and its significance.

(b) Explain why each channel in 8257 DMA controller is restricted to 16 K bytes of data transfer.

(c) Write instructions to generate a pulse every 100μs from Counter 0. Also, please specify
(i) the mode in which the Counter 0 has to be initialized and
(ii) the signal level of Gate 0 (High/Low).

**(2 +4) +2 +(2 + 1 + 1) = 12**

## Group – E

8. (a) What is the difference between the instruction MOV R0, #55H and MOV R0 , 55H? Describe the PSW register of 8051 microcontroller.

(b) Explain the interrupt system of 8051 microcontroller.

**(2 + 5) + 5 = 12**

(2+5) + (5) = 12

9. (a) Explain the internal RAM organization of 8051. Discuss how switching between register banks is possible. Give the sequence of instructions to switch from bank 0 to bank 2.

(b) What should be loaded in the TCON register to start timer 0 and timer 1?
How is the TMOD register modified to make each of the timers operate as counters?

**(3+ 2+ 3) + (2 + 2) = 12**

(3+2+3) + (2+2) = 12