MICROELECTRONICS & ANALOG VLSI DESIGN
(ECEN 3103)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) According to Moore's law, the dimensions of a MOS device are reduced with every technology node roughly by
(a) 50% (b) 60% (c) 70% (d) 80%.

(ii) Value of 'lambda' in 90nm technology node is
(a) 90nm (b) 45nm (c) 22nm (d) 11nm.

(iii) The threshold voltage _____ in short channel MOSFETs
(a) shifts towards lower voltage (b) shifts towards higher voltage
(c) remains same (d) none of the above.

(iv) Linear Region of an Ideal MOS Transistor can be modelled as a
(a) Resistance (b) Capacitance
(c) Current Source (d) Voltage Source.

(v) DI water is free from all traces of
(a) ionic contamination (b) particulate contamination
(c) bacterial contamination (d) all of the above.

(vi) Sputtering is a _____ process
(a) physical (b) chemical
(c) mechanical (d) none of the above.

(vii) Switched Capacitor Circuit realizes
(a) capacitance (b) resistance
(c) inductance (d) current sink.

(viii) Most Popular Scaling Technique in Today's Nano-Technology is
(a) Constant Voltage Scaling (b) Constant Field Scaling
(c) Constant Energy Scaling (d) Constant Charge Scaling.

(ix) The threshold voltage of a MOS depends on
(a) flat band voltage (b) depletion charge
(c) interface charge (d) all of the above.

(x) CMRR for a perfectly Matched Differential Amplifier Circuit is
(a) Zero (b) One (c) Infinite (d) None of above.

Group – B

2. (a) State Moore's law and mention the basic objectives of Integration.

(b) What is 'scaling'? What are the different theories of scaling of MOSFETs? Discuss their relative advantages and shortcomings.

2 + (2 + 3 + 5) = 12

3. (a) What is Constant Voltage Scaling and Constant Field Scaling.

(b) Which Scaling is more popular and why?

(c) Explain Short Channel Effects.

4 + 3 + 5 = 12

Group – C

4. (a) Mention the uses of SiO_2 in the Semiconductor fabrication industry.

(b) Differentiate between dry and wet oxidation. Write down the corresponding chemical equations.

(c) Prove that if a SiO_2 layer is grown by thermal oxidation, the thickness of Si consumed is 0.44 times the thickness of SiO_2. Given, the molecular weight of Si is 28.9 g/mol and the density of Si is 2.33 g/cm^3. The corresponding values for SiO_2 are 60.08 g/mol and 2.21 g/cm^3.

2 + 4 + 6 = 12

5. (a) Explain CMOS Fabrication flow step by step using self aligned N-Well Process Techniques.

(b) Draw the Structure of SOI and FINFET Transistors.

8 + 4 = 12

Group – D

6. (a) Explain how a CMOS switch can be used to overcome the dynamic range limitations associated with a single-channel MOS switch.

(b) Why does the gain of every MOS amplifier fall off at high frequencies? Draw the high-frequency equivalent circuit model for MOSFETs.

5 + (3 + 4) = 12

7. (a) Draw the Small Signal low frequency model for NMOS

(b) How MOS can be used as a Diode?

(c) Explain the operation of an NMOS Current Sink Circuit.

(d) Explain the Supply Voltage Divider Circuit by using NMOS Transistors.

3 + 3 + 3 + 3 = 12

Group – E

8. (a) Obtain the small signal equivalent circuit model of an active pmos load inverter.

(b) Find out its voltage gain and the output resistance.

6 + 6 = 12

9. (a) Consider a MOS differential amplifier with a differential input signal applied in a complementary manner. Show that the gain of the amplifier is doubled when the output is taken differentially and not in a single-ended fashion.

(b) Define CMRR.

10 + 2 = 12