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# Active-R tunable integrators using a current differencing buffered amplifier

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# Active-R tunable integrators using a current differencing buffered amplifier

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Some new active-R integrator realisation schemes using the transadmittance pole of a current differencing buffered amplifier (CDBA) element are presented. The time constant ($\tau$) is tunable by a single resistor whereas the integrator quality factor ($Q$) can be made very large with suitable realisability design. The active sensitivities of $\tau$ and $Q$ are extremely low. As an application, a variable frequency sinusoid oscillator utilising the integrators in a loop has also been designed. Practical results using the hardware implementation and by PSPICE macromodel simulation are included for a frequency range of 1 MHz $< f <$ 24 MHz.

**Keywords:** integrator; active-R circuit; CDBA



## Introduction

The current differencing buffered amplifier (CDBA) element is now being widely used as an active building block for the design of active-RC analogue function circuits (Acar and Ozoguz 1997, Salama, Ozoguz and Soliman 2001; Horng 2002; Tangsrirat, Surakampontorn and Fujji 2003; Keskin 2005; Gulsoy and Cicekoglu 2005; Nandi 2008); the element provides both voltage and current source output nodes and it is suitable for monolithic implementation with bipolar and CMOS technologies. The CDBA block can be implemented by a pair of AD-844 type current feedback amplifier (CFA) devices (Keskin 2005, Horng 2002); hence the advantageous features of the CFA, *viz*, high slew rate and improved bandwidth are preserved in the CDBA element. In the active-RC designs, the RC components may also be substituted by simulated-LR components (Nandi 1978) so as to derive dual circuit solutions. A wide-band WOBLER generator may be realised by using a d.c. voltage variable capacitance; for the same purpose in active-R designs, the tuner resistor can be replaced by a MOS transistor (Ananda Mohan 2004).

We propose here some active-R tunable integrators, using a single CDBA so that its z-node capacitance ($C_z$) is utilised and leads to new realisations suitable for applications to megahertz (MHz) ranges without requiring any external capacitor (Brand and Schaumann 1978; Sanyal, Sarker and Nandi 1990a). The advantages of such active based designs are known in the literature (Brand and Schaumann 1978; Nandi 1978; Ananda Mohan 2004), *viz*, elimination of external capacitors and

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enhancement of the usable frequency range. Although several CDBA based active-RC designs suitable for kilohertz (kHz) ranges are available (Horng 2002; Tangsrirat et al. 2003; Keskin 2005; Gulsoy and Cicekoglu 2005), such active-R single-tunable integrators have not yet been reported. Some experimental results in the frequency range of 1 MHz $< f <$ 24 MHz are included.

## 2. Analysis

The proposed integrators are shown in Figure 1 where the terminal properties of the CDBA are given by the matrix equation

$$\begin{pmatrix} i_z \\ v_w \\ v_a \\ v_b \end{pmatrix} = \begin{pmatrix} 0 & 0 & \alpha_a & -\alpha_b \\ \partial & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} v_z \\ i_w \\ i_a \\ i_b \end{pmatrix} \tag{1}$$

Analysis of Figure 1, assuming an ideal device ($\alpha_a = \alpha_b = \partial = 1$), yields

$$\begin{aligned} F_1(s) &\equiv V_0/V_1 = G_1/D(s) \\ F_2(s) &\equiv V_0/V_2 = -G_1/D(s) \end{aligned} \tag{2}$$

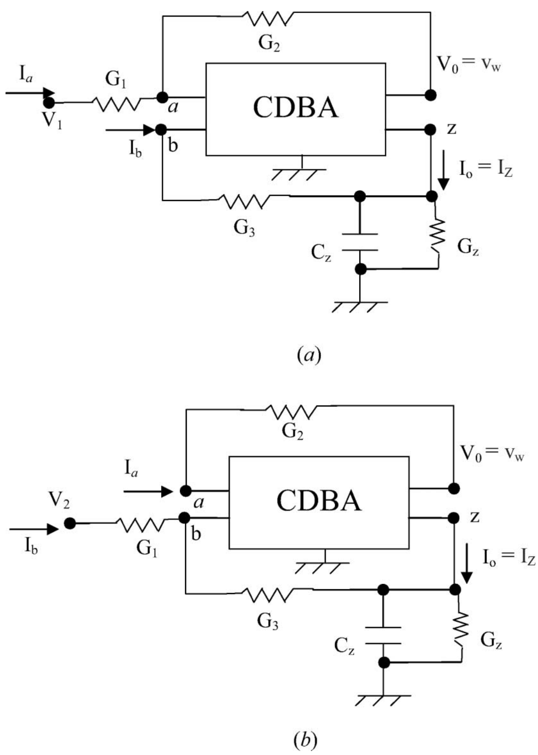



Figure 1. Proposed active-R integrators using the capacitive transadmittance component ($C_z$). (a) Non-inverting (b) inverting.

where

$$D(s) = \{2G_3 + G_z - G_2 + sC_z\} \tag{3}$$

Here $G_{1,2,3}$ denote the passive conductances and $G_z$ is the parasitic conductance at the $z$-node. Assuming an ideal CDBA, we get the realisability for ideal integrator function in both the circuits of Figure 1 as

$$G_2 = 2G_3 + G_z \tag{4}$$

From the datasheet (Analog devices 1990), one gets $G_z = 0.2\ \mu\Omega^{-1}$ and $C_z \approx$ 6 pF; hence $G_z$ may be neglected if the other resistors are chosen in k$\Omega$ ranges for tuning $C_z$ in MHz ranges. The other specifications of AD-844 are high unity gain bandwidth (60–600 MHz), high slew rate (2000 V/$\mu$s) and low offset voltage (100 mV). The time constant ($\tau$) for both the integrators is the same as $\tau = C_z R_1$. The modified realisability equation with a non-ideal device may be derived after postulating ($\alpha_a = \alpha_b = \partial \equiv (1 - \varepsilon)$ where $|\varepsilon|$ ($\ll$1) is finite non-zero) device port-tracking error (Horng 2002; Tangsrirat et al. 2003; Keskin 2005) given by

$$G_2 = (1 + 2\varepsilon)\{G_3(2 - \varepsilon) + G_z\} \tag{5}$$

and for both integrators, $\tau$ is altered as

$$\tau'/\tau = (1 + 2\varepsilon) \tag{6}$$

The active $\tau$-sensitivities are $S^{\tau} \approx \varepsilon/(1 + 2\varepsilon) \ll 1$. It may be noted that since the CDBA has $V_a = 0 = V_{\mathrm{b}}$ the $b$-node parasitics are bypassed to ground; the $a$-node has a low-value series parasitic resistance ($r_x \approx$ 30–40 $\Omega$) and its effect has been neglected (Cha, Ogawa and Watanabe 1998; Maundy, Sarkar and Gift 2006).

The quality-factor ($Q$) of the integrator (Brackett and Sedra 1976; Martin and Sedra 1977) is computed by expressing the transfer functions in the form $F(\omega) = (p + jq)^{-1}$ and then writing $Q = q/p$. We obtain

$$Q = \omega C_z R_3/[2 + R_3(G_z - G_2) + \varepsilon(2R_3G_2 - 1)] \tag{7}$$

If the realisability condition in Equation (5) is satisfied, we get an ideal integrator function with high quality ($Q \gg 1$) in both the circuits. It may be shown that the integrator quality is practically active–insensitive ($S^{Q} \ll 1$). Thus, while $\tau$ is variable with $R_1$, an appropriate value of $Q$ can be designed by selecting $R_3$, and the realisability condition of Equation (4) may be set by $R_2$ – all these adjustments could be done independently.

The aspect of microminiaturisation of such electronic function circuits with a view to process signals at higher speeds had been considered in the recent past. The design of integrators suitable for monolithic fabrication is quite useful to get high-quality high-frequency active filters (Ishibashi and Matsumoto 1994). To this end, a criterion for such performance, when fabricated in monolithic or hybrid IC technology may be estimated by the fractional changes in the circuit parameters ($\tau$, $Q$, $\omega_{\mathrm{o}}$) caused by environmental changes (e.g. temperature, ageing etc.).

These fractional changes (say for $Q$) can be written in terms of sensitivity $S^Q$ – summation and the incremental changes (Sanyal, Sarker and Nandi 1990b) in the RC components, given by

$$\partial Q/Q = \Sigma(S^Q_{R\mu})(\partial R_\mu/R_\mu) + \{S^Q_{Cz}(\partial C_z/C_z)\} \tag{8}$$

$\mu = 2{,}3{,}z$

After some calculations, we get $\Sigma(S^Q_{R\mu}) = 1 = S^Q_{Cz}$, hence

$$\partial Q/Q = (\partial R_\mu/R_\mu) + (\partial C_z/C_z) \tag{9}$$

In monolithic or hybrid IC technology, components of one kind track quite closely, i.e. fractional changes of all resistors (and capacitors) would be equal: $(\partial R\mu/R_\mu) = (\partial R/R)$ which yields

$$\partial Q/Q = (\partial R/R) + (\partial C_z/C_z) \tag{10}$$

It is possible to obtain resistor and capacitor components with equal but opposite temperature co-efficients in thin film technology, hence $\partial Q/Q = 0$.

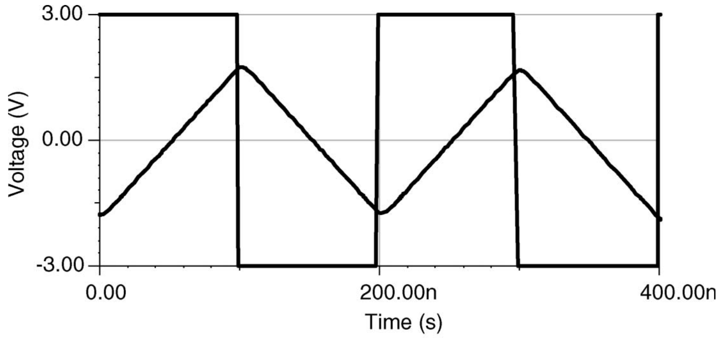
Next, we implemented a tunable sinusoid oscillator using a double-integrator loop for obtaining quadrature wave generation (Horng 2002). If the time constants are denoted by $\tau_{1,2}$ $(= C_{z1,2}\ R_{o1,2})$ for the two integrators, then the oscillation frequency is $\omega_o = (\tau_1\tau_2)^{-1/2}$ where both $\tau_{1,2}$ are single resistor controllable. The features of $\omega_o$ – tunability and the property of quadrature oscillation – had been experimentally verified; a typical 20 MHz waveform obtained by simulation (Macro model of AD844AN in PSPICE Library 1992) and the $f_o$-tunability range are shown next. The frequency stability factor (Wu, Liu, Hwang and Wu 1995; Nandi 2008) may be defined as $\{S_f \equiv \partial\theta/\partial u\}|_{u=1}$ where $u = (\omega/\omega_o)$ and $\theta$ is the loop phase shift; assuming identical integrators for simplicity and writing $n = (R_3/R_1)$ we obtained the stability factor

$$S_f = [1 + \{(G_1/\varepsilon)/(G_3 + 2G_2)\}]^{1/2} \approx [1 + (n/5\varepsilon)] \gg 1 \tag{11}$$

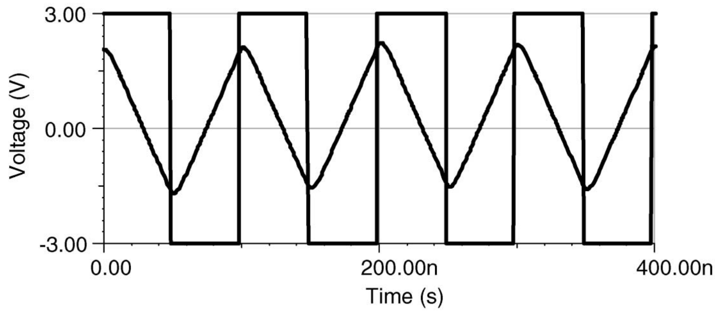
For relatively high frequency generation, we design $R_1 \ll R_3$, (i.e. $n \gg 1$); and because the device error is quite low ($\varepsilon \ll 1$), we observe that $S_f \gg 1$. A comparison of the $S_f$-values on some similar recent circuits may be seen as $S_f = 2/(1 + 2\varepsilon) \approx 2$ (Keskin 2005), $S_f = 1.3$ (Wu et al. 1995 ) and $S_f = \surd(n/\varepsilon) \gg 1$ (Nandi 2008). These findings are summarised in Table 1. However, our previous single CFA realisation (Nandi 2008) yields a better relative $S_f$-value by an order of $\surd 5$ with respect to the proposed design.

## Experimental results

Some measured results on conversion of square to triangular wave relative to the variation of $\tau$ through $R_1$ are shown in Table 2. With sine wave inputs, we observed a phase error of $\theta_e \leq 9^\circ$ from the nominal value of $\pm\pi/2$ at the higher end of test frequency of 24 MHz. Typical simulated responses of wave conversion are shown in Figure 2. The parasitic components had been measured as $C_z = 7.2$ pF




(*a*)




(*b*)

Figure 2. Simulation response of integrators using $R_3 = 60$ kΩ, $R_2 = 30$ kΩ and $C_z = 7.2$ pF (measured). (a) Non-inverting response at 5 MHz: $R_1 = 12.5$ kΩ, (b) Inverting response at 10 MHz: $R_1 = 6.3$ kΩ.

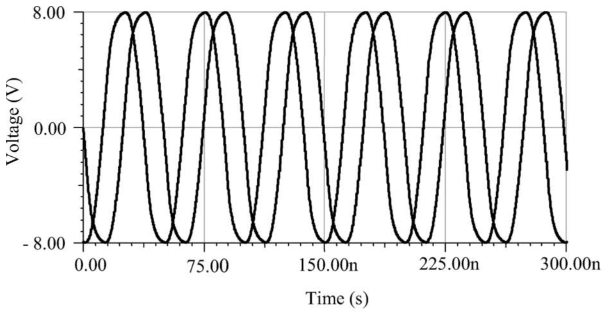


and $R_z = 4.8$ MΩ; other resistance values were calculated assuming a maximum value of deviations (Zeki and Kuntman 1997, Cha et al. 1998) as $\varepsilon = 10\%$ while taking $Q \approx 50$.

During experimentation, after observing the topological symmetry, we compounded the two structures of Figure 1 to obtain a dual-input ideal integrator with equal-value input resistors ($= R_1$); here however the single-tunability feature of $\tau$ could not be obtained. Nevertheless, this circuit exhibited excellent wave conversion and sinusoid frequency response characteristics with differential inputs; the phase error was measured to be 9° at about 20 MHz. We measured the common mode rejection ratio (CMRR) to be 96 dB with antiphase sinusoid excitation. The behaviour of this circuit was examined with different d.c. supply voltage levels at $\pm V_{cc} = 9$ V, 12 V, 15 V and 18 V; the power consumption (in mW) by the circuit at these levels were seen to be 108, 156, 170 and 210 respectively. Only very insignificant changes in the ramp slope ($\lambda$) and common mode gain could be observed.

The two integrators, considering $R_{o1}$ and $R_{o2}$ as their tuner resistors, were then connected in a regenerative loop for obtaining sinusoid generation. An experimentally generated sinewave at 20 MHz, along with its $f_o$-tuning characteristics, are shown in Figure 3a,b respectively. The circuit generated quadrature sinusoid signals at the two integrator outputs; quadrature oscillators are widely used in some telecommunication systems, e.g. quadrature mixers and single side band (SSB) modulators (Khan and Khawaja 2000).

It may be mentioned that the bandwidth of the current controlled current source (CCCS) type CDBA element is essentially determined by its transadmittance pole caused by the shunt $R_zC_z$ arm. The value of $R_z$ is usually quite high compared to



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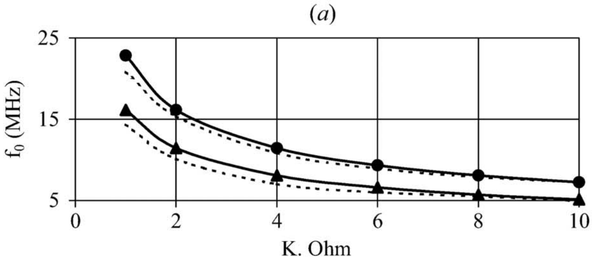

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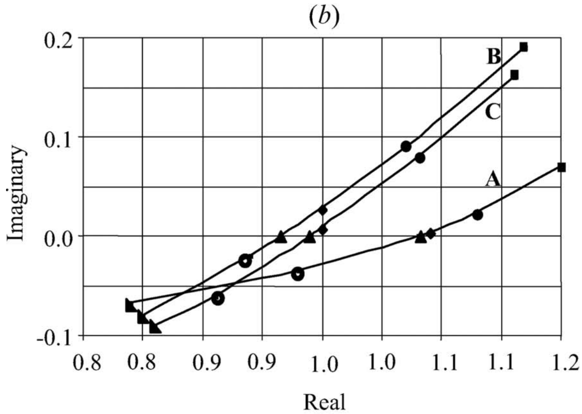

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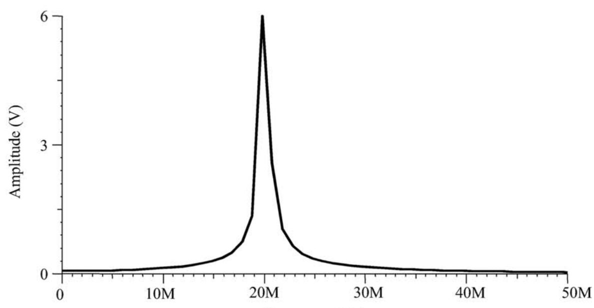

($d$)

Table 1. Comparison of $S_f$ for some recent oscillators.

| Ref. | Topology | $f_o$-tuning range reported (MHz) | $S_f$ |
|---|---|---|---|
| (Keskin 2005) | Active-RC | 0.1 | $2/(1+2\varepsilon) \approx 2$ |
| (Wu et al. 1995) | Active-R | 10.3 | $\approx 1.3$ |
| (Nandi 2008) | Active-R | 39.0 | $\sqrt{(n/\varepsilon)} \gg 1$ |
| Proposed | Active-R | 24.0 | $\sqrt{[1+(n/5\varepsilon)]} \gg 1$ |

Table 2. Measurement on the wave conversion characteristics of Figure 1a relative to $\tau$-variation by $R_1$.

| | | Slope $\lambda = v_0/t$ (volt/$\mu$s) of triangular wave | | | Linearity error (%) | |
|---|---|---|---|---|---|---|
| $R_1$ (k$\Omega$) | $\tau$ (ns) | Theoretical value | Simulation response | Hardware test | Simulation | Hardware |
| 10 | 72 | 41.67 | 42.5 | 40.2 | 2.00 | −3.52 |
| 20 | 144 | 20.83 | 20.2 | 19.8 | −3.04 | −4.96 |
| 30 | 216 | 13.89 | 13.8 | 13.1 | −0.64 | −5.68 |
| 40 | 288 | 10.42 | 10.5 | 8.7 | 0.80 | −16.48 |
| 50 | 360 | 8.33 | 8.5 | 7.8 | 2.00 | −6.40 |

Input excitation at 5 MHz with 6 $V_{pp}$ square wave.



other resistances in the circuit and hence may be neglected, whereas $C_z$ is the parasitic component that dictates the tuning characteristics in active-R designs at relatively high frequencies (Brand and Schaumann 1978). The Capacitance $C_z$ varies from its typical value from device to device and, during our hardware circuit test, we preferred to normalise it to a prescribed value after predistortion with a small external capacitance loaded to the $z$-terminal, e.g. the measured values were $C_{z1} = 6.8$ pF and $C_{z2} = 7.2$ pF; thereafter we loaded the $z$-terminals with 3.2 pF and 2.8 pF to obtain a normalised value of $C_{z1} = C_z = C_{z2} = 10$ pF for the oscillator design. The bias voltage for the CDBAs for this design had been chosen as $0 \pm 12$ V d.c.

Next, we measured the tuning error for the oscillator after evaluating the loop-function intersection of the real axis at phase cross-over point $(f|_{\theta=0^\circ})$ in a Nyquist plot in the vicinity of the oscillation frequency ($f_0$) as shown in

Figure 3. Double-integrator loop active-R oscillator response, $C_{z1} = C_z = C_{z2} = 10$ Pf. (a) Observed response at 20 MHz. (b) Tuning characteristics: ———— simulation; ............ hardware test; ●: $f_o$ *versus* $R_{o1}$ at $R_{o2} = 600\ \Omega$; ▲: $f_o$ *versus* $R_{o2}$ at $R_{o1} = 1$ k$\Omega$. (c) Nyquist plot of loop function $F_1F_2(s)$ measured in the vicinity of $u = 1 \pm 10\%$ with following symbols.

| $u \equiv f/f_o$ | 0.90 | 0.95 | 1.00 | 1.05 | 1.10 |
|---|---|---|---|---|---|
| *symbol* | ■ | ● | ◆ | ⊙ | ◣ |

▲ *indicates 0° phase cross-over point*

Nominal tuned frequency ($f_o$): A→10 MHz; B→15 MHz; C→20 MHz. (d) Frequency spectrum of the loop function $F_1F_2$(s) measured at tuned frequency of 20 MHz.

Table 3. Tuning error and THD measured at three different tuning frequencies.

| Curve | Tuned frequency $f_o$ (MHz) | $f\|_{\theta=0^\circ}$ (MHz) | $\Delta f$ (MHz) | Tuning error (%) | THD (%) |
|---|---|---|---|---|---|
| A | 10 | 10.04 | 0.04 | 0.4 | 4.6 |
| B | 15 | 15.40 | 0.40 | 2.6 | 5.5 |
| C | 20 | 20.12 | 0.12 | 0.6 | 6.9 |

Figure 3(c) for the three tuning frequencies at 10 MHz, 15 MHz and 20 MHz; the errors are seen to be quite low as listed in Table 3. The frequency spectrum for $f_0 = 20$ MHz is shown in Figure 3(d). We also measured the total harmonic distortion (THD %) of the generated sinusoids at these frequencies; these are indicated in Table 3.

## Conclusion

Using the capacitive transadmittance element of a CDBA, two new tunable active-R ideal integrators are presented. Application of the integrators to variable frequency sinusoid wave generation using the double-integrator loop is proposed. The responses of these circuits have been verified in a range of 1 MHz $< f <$ 24 MHz by both hardware tests and by PSPICE simulation. The proposed configurations offer good quality low-sensitivity functional performance measured at relatively high frequency and hence would be suitable for its use as a building block in various analogue signal processing and filtering applications (Chiang 1986; Kerwin Huelsman and Newcomb 1967; Nandi, Goswami, Nagaria and Sanyal 2003) using the CDBA and only a few resistors. Some possible further applications of the proposed integrator and wave generator may be in areas of environmental solutions towards identification of damage in tree wood and detection of humans trapped in heavy snow or sandstorms.

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## References

Acar, C., and Ozoguz, S. (1997), ‘A Versatile Active Building Block: Current Differencing Buffered Amplifier Suitable for Analog Signal Processing Filters’, *Microelectronics Journal*, 30, 157–160.

Analog devices. (1990), *Linear Products Databook*, MA, USA: Norwood.

Ananda Mohan, P.V. (2004), *Current Mode VLSI Analog Filters*, Birkhausser, Switzerland: Springer.

Brackett, P.O., and Sedra, A.S. (1976), ‘Active Compensation for High-Frequency Effects in Op-Amp Circuits with Applications to Active-RC Filters’, *IEEE Transactions, Circuit and Systems*, CAS-23, 68–72.

Brand, J.R., and Schaumann, R. (1978), ‘Active-R Filters: Review of Theory and Practice’, *IEE Proceedings(G), Electronic Circuits and Systems*, 2, 89–101.

Cha, H.W., Ogawa, S., and Watanabe, K. (1998), ‘Class-A CMOS Current Conveyor’, *IEICE Transactions*, E-81A, 1164–1167.

Chiang, H.H. (1986), *Electronic Waveforming and Processing*, New York: Wiley.

Gulsoy, M., and Cicekoglu, O. (2005), ‘Lossless and Lossy Synthetic Inductors Employing Single Current Differencing Buffered Amplifier’, *IEICE Transactions*, E88-B, 2152–2155.

Horng, J.W. (2002), 'Current Differencing Buffered Amplifiers Based Single Resistance Controlled Quadrature Oscillator Employing Grounded Capacitors', *IEICE Transactions*, E85-A, 1416–1419.

Ishibashi, Y., and Matsumoto, F. (1994), 'Realization of a Monolithic Integrator with Improved High-Frequency Response Using a Miller Integrator and its Application to Filters', *Electronics & Communications in Japan, Part-III: Fundamental Electronic Science*, 77, 97–105.

Kerwin, W.J., Huelsman, L.P., and Newcomb, R.W. (1967), 'State Variable Synthesis for Insensitive Integrated Circuit Transfer Function', *IEEE Transactions, Solid State Circuits*, SC-2, 87–92.

Keskin, A.U. (2005), 'Voltage Mode High-Q Bandpass Filters and Oscillators Employing Single CDBA and Minimum Number of Components', *International Journal of Electronics*, 92, 479–487.

Khan, I.A., and Khawaja, S. (2000), 'An Integrable $g_m$-C Quadrature Oscillator,' *International Journal of Electronics*, 87, 1353–1357.

*Macromodel of AD844AN in PSPICE Library*, (1992). California, USA: Microsim Corporation.

Martin, K., and Sedra, A.S. (1977), 'On the Stability of Phase-Lead Integrator', *IEEE Transactions, Circuit and Systems*, CAS-24, 321–324.

Maundy, B.J., Sarkar, A.R., and Gift, S.J. (2006), 'A New Design for Low Voltage CMOS Current Feedback Amplifiers', *IEEE Transactions, Circuit and Systems(II), Express Brief*, 53, 34–38.

Nandi, R. (1978), 'Active-R Realization of Bilinear RL Impedances and their Applications in a High-Q Resonator and External Capacitorless Oscillator', *IEEE Proceedings*, 66, 1666–1668.

Nandi, R. (2008), 'Tunable Active-R Oscillator Using a CFA', *IEICE Electronics Express*, 5, 248–253.

Nandi, R., Goswami, A., Nagaria, R.K., and Sanyal, S.K. (2003), 'Voltage Tunable Differential Integrator and Differentiator Using Current Feedback Amplifier,' *IEICE Transactions*, E86-C, 2329–2331.

Salama, K., Ozoguz, S., and Soliman, A. (2001), 'A New Universal Biquad Using CDBAs', in *Proceedings of Midwest Symposium, Circuits and Systems* (MWSCAS), IEEE Explore, USA, Vol. 2, pp. 850–853.

Sanyal, S.K., Sarker, U.C., and Nandi, R. (1990a), 'A Novel Microprocessor Controlled Active-R Multifunction Network: Design of Programmable Filter, Oscillator and FSK/PSK Wave Generator', *IEEE Transactions, Circuit and Systems*, 37, 1085–1091.

Sanyal, S.K., Sarker, U.C., and Nandi, R. (1990b), 'Increased Time Constant Dual-Input Integrators', *IEEE Transactions, Instrumentation and Measurement*, IM-39, 672–673.

Tangsrirat, W., Surakampontorn, W., and Fujji, N. (2003), 'Realization of Leapfrog Filters Using Current Differencing Buffered Amplifiers', *IEICE Transactions*, E86-A, 318–326.

Wu, D.S., Liu, S.I., Hwang, Y.S., and Wu, Y.P. (1995), 'Multiphase Sinusoidal Oscillator Using the CFOA Pole', *IEE Proceedings (G)*, 142, 37–40.

Zeki, A., and Kuntman, H. (1997), 'Accurate and High Input Impedance Current Mirror Suitable for CMOS Current Output Stages', *Electronics Letters*, 33, 1042–1043.