B.TECH/EE/3RD SEM/ELEC 2101/2018
ANALOG & DIGITAL ELECTRONIC CIRCUITS
(ELEC 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) To avoid false triggering, the RESET pin of 555 timer is generally connected to
(a) $+V_{cc}$ (b) $-V_{cc}$ (c) Ground (d) Trigger.

(ii) An ideal regulated power supply should have regulation equal to
(a) zero (b) 50% (c) 100% (d) 25%.

(iii) The octal equivalent of $(1001101.1011)_2$ is
(a) 114.54 (b) 115.54 (c) 115.45 (d) 115.56.

(iv) A flip flop is called a latch when it is
(a) edge triggered (b) level triggered
(c) both (a) and (b) (d) without any trigger.

(v) The output of a logic gate is 1 when all its inputs are at logic zero. The gate is either
(a) a NAND or an EX-OR (b) an OR or an EX-OR
(c) an AND or an EX-OR (d) a NOR or an EX-NOR.

(vi) The output of an integrator circuit with square wave input is
(a) Triangular wave (b) Impulse
(c) Parabola (d) Step.

(vii) The bandwidth of an ideal op amp is
(a) Infinity (b) 1 MHz (c) 0 Hz (d) 10 Hz.

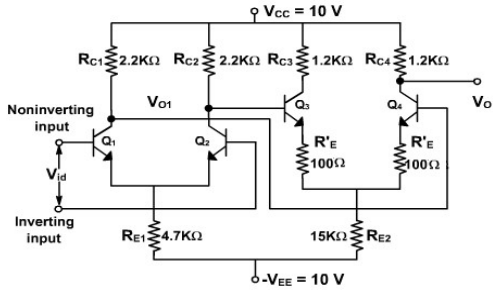
(viii) Which is the necessary condition of gain while designing Wien bridge oscillator to ensure sustained oscillations?
(a) A ≥ 3 (b) A ≥ 2 (c) A ≥ 29 (d) A ≥ 1.

(ix) The minimum number of flip flops required to design a MOD-10 counter is
(a) 03 (b) 10 (c) 04 (d) 05

(x) The Boolean expression $\overline{A}\overline{B}C\overline{D}$ is a
(a) a sum term (b) a product term
(c) a literal term (d) always 1

Group – B

2. (a)

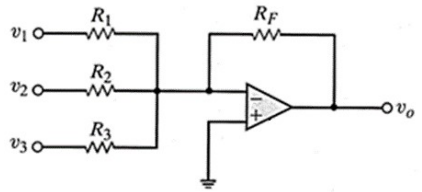


Assume V_{BE} = 0.7V and β = 100 for all the transistors used
Determine: i) collector current in each transistor
ii) collector to emitter voltage for each transistor
iii) output voltage V_o
iv) input resistance
v) output resistance

(b) Show that the input resistance with feedback R_{if} for a voltage series feedback amplifier is given by:
$R_{if} = R_i(1 + A\beta)$
Where R_i is the input resistance without feedback, A is the open loop gain and β is the gain of the feedback circuit.

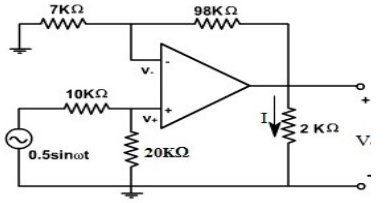
8 + 4= 12

3. (a) Derive the expression of output voltage for the circuit.
Hence determine the output voltage considering R_1 = 1kΩ, R_2 = 5kΩ, R_3 = 2kΩ and R_F = 1.5kΩ.The input voltages are V_1 = 1V, V_2 = 5V and V_3 = 2V



(b) Realise the linear differential equation using minimum number of Op amps.
$\frac{d^2y}{dt^2} + 4\frac{dy}{dt} + 2y = 5$

(c) Determine the output voltage Vo and determine the current I through 2kΩ resistor



(2 +2) + 4 + 4 = 12

Group – C

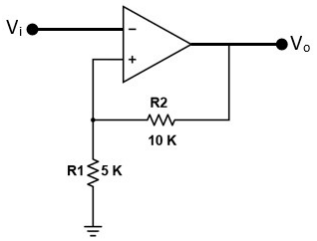
4. (a) Draw a neat diagram of phase shift oscillator. Derive the expression of oscillation frequency. Also determine the gain at the oscillation frequency.

(b) Design a series voltage regulator using an operational amplifier and a 6V zener diode to maintain a regulated output of 24V. Assume that the unregulated input varies between 20V and 30V and that the current through the zener diode must be at least 20 mA to keep it in its breakdown region.

(1+ 4+ 4) + 3 = 12

5. (a) Show that the duty cycle of an astable multivibrator using op amp is 50%

(b) In the figure the input voltage V_i is a symmetrical sawtooth wave with average value zero, a positive slope and peak to peak value of 20V. If the peak to peak voltage of the output is 30V, draw the output waveform. Compute the average value of the output.



(c) Using 7805C voltage regulator design a current source that will deliver 0.25A current to 48Ω, 10W load.

6 + (2 + 1) + 3 = 12

$6 + (2+1) + 3 = 12$

Group – D

6. (a) Simplify the Boolean expression using Karnaugh map technique:
$F = \sum m(1,5,6,12,13,14) + \sum d(2,4)$
Also implement the circuit using suitable logic gates.

(b) Prove that $\bar{A}C\,[\overline{\bar{A}BD}] + \bar{A}B\bar{C}\bar{D} + AB\bar{C} = B\bar{C} + \bar{A}\bar{D}(B + C)$

(c) Design a full subtractor using NAND gate only.

6 + 3 + 3 = 12

7. (a) Form a multiplexer tree to give a 16×1 MUX from two 8×1 MUX.

(b) Design the logic circuit of a BCD to decimal decoder. Explain its function.

(c) Expand the following expression to a standard SOP form: Y=AB+ACD

5 + 4 + 3 = 12

Group – E

8. (a) Explain the operation of a 3 bit asynchronous Up Counter using JK flip flop. Draw the waveforms.

(b) Design a 4 bit SISO shift register using D flip flop and explain its operation for right shift mode.

6 + 6 = 12

9. (a) Perform the conversion of D flip flop to JK flip flop.

(b) What is race around condition? How it can be overcome?

(c) Explain how JK flip flop can be used as a frequency divider.

5 + 4 + 3 = 12