B.TECH/CSE/5TH SEM/CSEN 3104/2018
COMPUTER ARCHITECTURE
(CSEN 3104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The number of cycles required to complete n tasks with k-stage pipeline is
(a) k+n-1 (b) k (c) nk+1 (d) none of the above.

(ii) A 64-input Omega Network requires how many stages of 2 × 2 switches?
(a) 6 (b)64 (c) 8 (d) 4.

(iii) Stride in vector processor is used to
(a) differentiate different data types (b) registers
(c) differentiate different data (d) None of the above.

(iv) For two instructions I and J WAR hazard will occur, if
(a) $R(I) \cap D(J) \neq \varnothing$ (b) $R(I) \cap R(J) \neq \varnothing$
(c) $D(I) \cap R(J) \neq \varnothing$ (d) none of the above.

(v) There is a pipeline with four stages. The number of instructions is 40. What will be the approximate speed-up of this circuit?
(a) 1 (b) 2 (c) 3 (d) 4.

(vi) Cache memory
(a) increases performance (b) decreases performance
(c) increases machine cycle (d) none of the above.

(vii) Zero address instruction format is used for
(a) RISC architecture (b) CISC architecture
(c) Von-Neumann architecture (d) stack-organized architecture.

(viii) Which of the following is not a property of a memory module?
(a) inclusion (b) consistency
(c) capacity (d) commutative.

(ix) Which of the following is an example of 2-dimensional topologies in static network?
(a) Mesh (b) $3C^3$ Network
(c) Linear Array (d) None of the above.

(x) SIMD represents an organization that _____.
(a) refers to a computer system capable of processing several programs at the same time.
(b) represents organization of single computer containing a control unit, processor unit and a memory unit.
(c) includes many processing units under the supervision of a common control unit
(d) none of the above.

Group – B

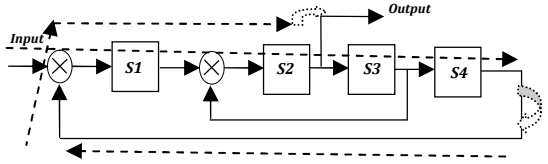
2. (a) Differentiate between Von Neuman and Harvard architecture; explain with schematic diagram.

(b) "Instruction execution throughput increases in proportion with the number of pipeline stages". Is it true? Justify your statement.

(c) How can hazard occur in executing the following set of instructions?
I1: MOV R1,A ; [A] <- (R1)
I2: ADD R2,R3; R3 <- (R3) + (R2)
I3: SUB R4,R5; R5 <- (R4) – (R5)
I4: NOP
All the symbols have their usual meanings. You may assume a pipeline unit consisting of four stages.

4 + 4 + 4 = 12

3.



(a) Consider the above pipelined processor with four stages. This pipeline has a total evaluation time of six clock cycles. All successor stages must be used after each clock cycle.

(b) Specify the reservation table for this pipeline with six columns and four rows following the dotted data path.

(c) List the set of forbidden latencies between task initiations.

(d) Draw the state diagram.

(e) List all simple cycles from state diagram.

(f) List all greedy cycles from the state diagram.

(g) Determine the minimal average latency (MAL).

(h) What are the upper and lower bound of MAL?

3 + 1+ 3+ 1+ 2+ 2 = 12

Group – C

4. (a) Explain vector stride and strip mining using examples.

(b) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node101 simultaneously in a 8×8 Omega network. Does blocking exist in this case?

(c) Show how the following two matrices can be multiplied using ILLIAC-IV network.

$$\begin{bmatrix} 1 & 2 \\ 4 & 5 \end{bmatrix} \qquad \begin{bmatrix} 4 & 7 \\ 7 & 6 \end{bmatrix}$$

3 + (2+2+1) + 4 = 12

5. (a) Explain multistage implementation of a cube network with a suitable diagram.

(b) Implement data routing logic of SIMD architecture to compute

$$s(k) = \sum_{i=0}^{k} A_i \text{ for } k=0.\ 1,2,.....N-1$$

(c) You have the following instruction stream coming into a chained vector processor

Load VR , A[3:0]
Add VR , #1
Mul VR , #2
Store A[3:0] , VR

A is a vector of length 4. VR is a vector register.

Show how the above code is executed in a vector processor with four pipeline stages (Load / Add / Multiply and Store).

4 + 5 + 3 = 12

Group – D

6. (a) Compare the relative performance (ideal speedup) of a superscalar processor with that of a base scalar machine, given N independent instructions, k stages and m – issue superscalar machine.
Explain the speedup limit.

(b) Explain the pipelining in superscalar processor. Give two reasons that limit the degree m of superscalar processor to 2 to 5.

(5 + 1) +(4 + 2) = 12

7.(a) Consider the following program: (assume Opcode <srec>,<dest> format):

```
Add R3, R2
Sub R3,R4
Add R2,R1
Mov R1,[R4] ; writes to memory location
            ; pointed to by R4
Jnz R1, ThisPlace
: : :       : : :
ThisPlace: <some code>
```

Assuming a delay slot value of 3, rewrite the code to exploit the delayed branching mechanism. Explain briefly how performance is improved because of application of the above technique.

(b) Suppose that in an MIMD system, there are 20 processors. Each has its own cache. Suppose two processors each caches a single shared variable X. How many messages are sent across the system for maintaining cache coherency of X if a) snooping protocol is used? b) If a centralized directory based protocol is used? Explain your answer.

(c) Explain why memory-to-memory architecture is not possible in an array or vector processor architecture.

5 + 4 + 3 = 12

Group – E

8. (a) Draw a data flow graph for approximate calculation of
$\cos x \approx 1 - x^2 / 2! + x^4/4! - x^6/720$

What are the advantages and disadvantages of the data flow architecture?

(b) Explain the concept of VLIW architecture, highlighting how it is different from instruction level parallelism. What are the reasons behind VLIW concept failing to fulfill its promise?

(4 + 4) +(3 + 1) = 12

9. (a) What is cache coherence problem? Suggest methods used to solve cache coherence problem.

(b) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts :

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmetic	50,000	2
Data Transfer	70,000	3
Floating Point Arithmetic	25,000	1
Branch	4,000	2

Calculate the effective CPI, MIPS rate and execution time for this program

(2 + 4) + 6 = 12