VLSI DESIGN AUTOMATION
(ECEN 4181)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) For Sub Micron Technology L_{gate} (Channel Length) is
(a) > 100 nm (b) < 100 nm
(c) > 1um (d) None of these.

(ii) Output of physical design is
(a) Circuit (b) Layout
(c) Logical Model (d) RTL Schematic.

(iii) Ideal Current Source has Resistance of value
(a) 0 ohm (b) Infinite
(c) 100 K ohm (d) 10 ohm.

(iv) The HDL used for industrial purpose is
(a) SPECTRA (b) PSPICE
(c) VERILOG (d) MATLAB.

(v) Most popular interconnect material is
(a) Gold (b) Silver
(c) Aluminium (d) Silicon Dioxide.

(vi) For a Standard Cell Layout
(a) Height is fixed (b) Width is fixed
(c) Both Height and Width are fixed (d) None of Above.

(vii) Finite State Machine is normally done using _____ Method.
(a) Full Custom (b) FPGA
(c) Std Cell based Semi Custom (d) Gate Array

(viii) MOS Transistor has below number of terminals
(a) 1 (b) 2
(c) 3 (d) 4.

(ix) NMOS Transistor in linear region can be modelled as
(a) Resistance (b) Current Source
(c) Open Circuit (d) Voltage Source.

(x) Stick diagram helps _____
(a) Logic Design (b) Circuit Design
(c) Layout Design (d) Architecture Design.

Group – B

2. (a) What is the issue related to NMOS based Inverter Design?
(b) How is the issue fixed using CMOS based Inverter?

6 + 6 = 12

3. (a) What are various Capacitance Components of a MOS Transistor?
(b) Draw VTC (Voltage Transfer Curve) of CMOS Inverter.
(c) For a CMOS Inverter V_{OH} = 5V, V_{OL} = 0V, V_{IH} = 3.4V, V_{IL} = 2.2V. What is the Value of NM_H and NM_L **?**

4 + 4 + 4 = 12

Group - C

4. (a) What is function of a Latch?
(b) Implement Latch using Digital Gate.
(c) What is function of a Flip-Flop?
(d) How Flip Flop can be implemented using Latch?

3 + 3 + 3 + 3 = 12

5. (a) Draw Flow Diagram of VLSI Design Cycle.
(b) Draw Flow Diagram of Front End Design Flow.
(c) Write Verilog behavioural model for a D –Flip Flop.

4 + 4 + 4 =12

Group - D

6. (a) Draw flow diagram of High Level Synthesis.
(b) Draw flow diagram of Logic Synthesis.
(c) Draw BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a $\leq$ b$\leq$ c.
(d) Create ROBDD Diagram and corresponding optimized Boolean expression.

3 + 3 + 3 + 3 = 12

7 (a) For Floorplanning problem, what are inputs, outputs and Objective (Cost) function ?
(b) Write problem formulation of Global Routing using Steiner Tree.

6 + 6 = 12

Group - E

8. (a) Write Verilog code of Behavioural Modelling of a 3 input NOR gate.
(b) Draw Flow Diagram of High Level Synthesis.

6 + 6 = 12

9. Write short notes on the following:
(i) Left Edge Algorithm for Detailed Routing.
(ii) Technology Mapping Algorithm using DAG.

6 + 6 = 12