COMPUTER ARCHITECTURE
(INFO 3102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) An architecture in which data is sent in a rhythmic fashion is known as
(a) systolic array (b) linear array
(c) chordal ring (d) none of these.

(ii) What will be the speed-up for a 6-segment linear pipeline when the number of instruction n = 100?
(a) 4.5 (b) 3.82 (c) 5.71 (d) 9.12.

(iii) When block size is equal to entire cache size, then hit ratio becomes
(a) 1 (b) 2 (c) 0 (d) 4.

(iv) In which type of memory mapping there will be conflict miss?
(a) Direct mapping (b) Set associative mapping
(c) Associative mapping (d) both (a) and (b).

(v) A mesh is an example of
(a) dynamic network (b) static network
(c) switch (d) Omega network.

(vi) Prefetching is a solution for
(a) data hazard (b) structural hazard
(c) control hazard (d) none of these.

(vii) Systolic array is an example of _____ architecture.
(a) MIMD (b) MISD (c) SIMD (d) SISD.

(viii) The number of instructions to be executed in a program is called
(a) cycle (b) time period
(c) instruction count (d) none of these.

(ix) In general 128-input Omega network requires _____ 2 × 2 switches
(a) 8 (b) 7 (c) 6 (d) 64.

(x) A broadcast operation, known as request for Ownership is used by
(a) compiler based protocol (b) snoopy protocol
(c) directory protocol (d) MESI protocol.

Group – B

2. (a) Differentiate between static and dynamic scheduling. What is pipeline hazard?

(b) Show that the performance of pipeline degrades by 46% with the inclusion of branching effect.

(c) State the concept of internal forwarding and discuss its types. How does it differ from register tagging?

(4 + 1) + 3 + (3 + 1) = 12

3. (a) A 50 MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts.

Instruction Type	Instruction Count	Clock Cycle Count
Arithmetic	50000	3
Data Transfer	25000	4
Floating Point	20000	2
Control Transfer	5000	2

Determine the effective CPI, MIPS rate and execution time of the program.

(b)

	1	2	3	4	5	6	7
S1	X			X			X
S2		X			X		
S3			X			X	
S4				X	X		

Determine the collision vector. Draw the state transition diagram. Find out the greedy cycle for each state. Calculate MAL, its upper bound and lower bound.

(c) What is arithmetic pipeline?

3 + (2 + 2 + 2 + 2) + 1 = 12

Group – C

4. (a) A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16384 blocks and each block contains 256 eight bit words.

(i) How many bits are required for addressing the main memory?
(ii) How many bits are needed to represent the sub-fields of virtual address?

(b) Explain victim cache and loop fusion.

(c) "Multi-level cache can reduce effective memory access time" — explain with example.

(3 + 3) + (2 + 2) + 2 = 12

5. (a) Based on the following information calculate the average access time of the computer system.
Number of entries in the TLB = 16
TLB search time = 150 ns
Main memory access time = 10 ns
TLB hit ratio = 0.75

(b) "If the TLB and cache memory are working together, then the effective memory access time will be reduced" — justify.

6 + 6 = 12

Group – D

6. (a) Discuss the working of VLIW processor in detail with suitable diagram. State the advantages and disadvantages of VLIW processor.

(b) What is instruction level parallelism (ILP)? Explain any two techniques that can be used for improving ILP with suitable examples as necessary.

(4 + 4) + (1 + 3) = 12

7. (a) Discuss the types of vector instruction and its format.

(b) Discuss in detail the microprogrammed control unit.

(c) What is array processor? Discuss the architectures of array processor.

4 + 4 + (1 + 3) = 12

Group – E

8. (a) Explain the factors that influence the block size selection in DSM.

(b) Explain the following memory consistency models with examples.
(i) Sequential consistency model (ii) Causal consistency model (iii) Processor consistency model (iv) Release consistency model.

(c) What is clustering? State the classifications of clusters.

4 + 4 + (1 + 3) = 12

9. (a) Design a 4D hypercube network. What are multistage switching networks?

(b) Draw data flow graph to represent the following computations:
(i) A = P + Q
(ii) B = A / Q
(iii) C = P * A
(iv) D = C / A
(v) E = D - C

(c) Explain MESI cache coherence protocol in detail.

(3 + 1) + 4 + 4 =12