B.TECH/IT/3RD SEM/INFO 2101/2018
DIGITAL ELECTRONICS
(INFO 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The main difference between a register and a counter is as follows.
(a) A register has no specific sequence of states
(b) A counter has no specific sequence of states
(c) A register has capability to store one bit of information but counter can store n bits.
(d) None of the above.

(ii) How many flip-flops are required to construct a decade counter?
(a) 4 (b)8 (c) 5 (d) 10.

(iii) Internal propagation delay of asynchronous counter is removed by
(a) ripple counter (b) ring counter
(c) modulus counter (d) synchronous counter.

(iv) The operation of multiplexer is same as
(a)OR-AND operation (b) AND-OR operation
(c)OR-NAND operation (d) None of the above.

(v) How many select lines are contained in a MUX with 1024 input lines and 1 output line?
(a) 64 (b) 10 (c)128 (d) 256.

(vi) The logic family which has highest noise margin is:
(a) TTL (b) CMOS (c) RTL (d) ECL.

(vii) The ADC used in digital voltmeter is:
(a) dual slope type (b) ramp type
(c) successive approximation type (d) counter type.

(viii) The 9's complement of the number 45 is
(a) 22 (b) 23 (c) 24 (d)54.

(ix) The NAND-NAND realization is equivalent to :
(a) AND-NOT (b) OR-NOT (c) AND-OR (d)NOT-OR.

(x) Data distributers are basically same as
(a) decoder (b) demultiplexer (c) multiplexer (d) priority encoder.

Group – B

2. (a) Perform subtraction of BCD numbers: (64 – 25) using 9's complement.

(b) Simplify the following logic function using Karnaugh Map :
$f=\prod M(1,5,6,7,11,12,13,15)$.
Identify the PI by using Quine-McCluskey method for the following function :
$F(A,B,C,D)=\sum m(0,1,2,5,6,7)$.

4 + (4 + 4) = 12

3. (a) Find the possible bases in arithmetic operation:
(i) $51/3=13$ (ii) $(292)_{10} = (565)_R$
Given that , $AB' + A'B = C$, Prove that: $AC' + A'C = B$.

(b) Minimize the following switching function to the simplest possible POS forms: $F(A,B,C,D)= (2,3,4,5,14,15)+ \sum d(10,11,12,13)$, where d denotes don't care condition.

(4 + 2) + 6 =12

Group – C

4. (a) A combinational circuit is given by $f(w,x,y,z) = xy + wxy + z'$. Design the circuit using decoder and OR gates.

(b) Design 4- bit BCD to XS-3 converter.

5 + 7 =12

5. (a) Explain the working principle of BCD Adder with suitable diagram.

(b) Explain the operation principle of 2- bit comparator circuit.

7 + 5=12

Group – D

6. (a) Explain S-R flip-flop using proper logic diagram and truth table.

(b) Design a mod–11 down counter using J-K flip-flops and show the output using timing diagram.

4 + 8 = 12

7. Design a 10011 sequence detector using D flip-flop. Allow overlap.

12

Group – E

8. (a) Explain the working principle of 3-bit Flash ADC with suitable diagram.

(b) The logic levels used in a 4-bit R-2R ladder DAC are: 1=5V and 0=0V.Find the output voltage for input 1111.You must show the complete derivation for the expression of output voltage.

6 + (2 + 4) = 12

9. (a) Find the successive-aproximation ADC output for a 4-bit converter to a 4.67 V input if the reference voltage is 15 V.

(b) Compare maximum conversion time of a 10-bit digital ramp ADC with that of a successive approximation ADC both using a clock of 1 MHz. Define the terms: propagation delay, figure of merit.

5 + (3 + 4) = 12