M.TECH/VLSI/2ND SEM/VLSI 5241/2018

LOW POWER VLSI CIRCUIT AND SYSTEM
(VLSI 5241)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Maximum Power saving is possible in
(a) system level (b) architecture level
(c) transistor level (d) gate level.

(ii) If threshold voltage of transistor is increased 2x, dynamic power of digital gate
(a) decreases 2x (b) increases 2x
(c) remains same (d) increases 4x.

(iii) Activity Factor is maximum for which of the following circuit outputs?
(a) Memory Node (b) Dynamic
(c) Static (d) Clock.

(iv) If P_A is the signal probability of A- input of an inverter, Then signal probability of the inverter output is
(a) P_A (b) $1-P_A$ (c) 1 (d) 0.25.

(v) Maximum leakage power contribution comes from
(a) channel leakage
(b) gate leakage of ON Transistor
(c) junction leakage
(d) gate leakage of OFF Transistor.

(vi) Memory Cell with Maximum leakage is
(a) SRAM Cell (b) DRAM Cell
(c) Latch Cell (d) Flip Flop Cell.

(vii) Maximum Leakage reduction in ROM array is possible with
(a) all '0' bits in array (b) all '1' bits in array
(c) 50% '0' bits in array (d) 75% '0' bits in array.

(viii) If Rise Time of input of an inverter is increased, then Short Circuit Current
(a) increases linearly (b) decreases linearly
(c) remains same (d) decreases exponentially.

(ix) Both Power and Delay Reduction for a Digital Gate is possible if
(a) C_L decreases (b) V_{DD} decreases
(c) Activity factor decreases (d) never possible.

(x) Which of the following logic family has the maximum power dissipation?
(a) Static CMOS
(b) Dynamic with high activity
(c) Pseudo NMOS
(d) Dynamic with low activity.

Group - B

2. (a) If P_A and P_B are signal probability of A and B-input of an AND gate, calculate transition probability of output Y of the NAND gate.

(b) Explain Glitch Power of a Digital Circuit with an example and show how that can be reduced with same example.

6 + 6 = 12

3. (a) Under what input condition Channel Leakage Power through a 3-input NAND Gate is minimum and why ?

(b) Draw Gate Delay vs Threshold voltage curve for various supply voltage of a digital gate and explain the variation.

6 + 6 = 12

Group - C

4. (a) What are the various components of Load Capacitance (C_L) in Digital Circuit ?

(b) What are the various techniques of reducing C_L to reduce power ?

6 + 6 = 12

5. (a) What are the various techniques of Dynamic Power reductions by changing Power Supply (V_{DD})?

(b) Define Short Circuit Power in VLSI Circuit and Explain the short Circuit Power Reduction Techniques.

6 + 6 = 12

Group - D

6. (a) Explain how transistor stacking effect can reduce channel leakage significantly.

(b) How high-K plus Metal-gate Transistor reduces gate leakage significantly compared to traditional Silicon Dioxide insulator plus Poly-gate Transistor ?

6 + 6 = 12

7. (a) What is Short Circuit Power in VLSI Circuit and how short Circuit Power can be reduced ?

(b) Assuming same throughputs, which architecture is better between the parallel and pipeline architectures from power and area perspective and why? Explain with example.

6 + 6 = 12

Group - E

8. (a) Under what condition Dynamic logic gates can provide less power with respect to Static CMOS gates? Explain with example.

(b) How Power reduction is possible from 3 Transistor DRAM cell array to 1 Transistor DRAM cell array? Explain with circuit diagram .

6 + 6 = 12

9. (a) Draw Circuit Diagram of 6 Transistor SRAM cell with appropriate interface signals and show sources of various leakage power in SRAM cell .

(b) Why pseudo NMOS logic family is not power friendly ?

6 + 6 = 12