(b) Explain why Double Gate (DG) MOSFETs have better immunity to the Short Channel Effects?

**6 + 6 = 12**

**Group - E**

8. (a) What is modulation doping? What are its benefits?

   (b) Explain how modulation doping is used in MODFETs.

**(2 + 2) + 8 = 12**

9. Write short notes on the following:
   i. Volume inversion in DG-MOSFETs.
   ii. Random Dopant Fluctuation.

**(2 × 6) = 12**



# M.TECH/VLSI/2ND SEM/VLSI 5231/2018

## ADVANCED MICRO & NANO DEVICES
## (VLSI 5231)

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

**Group – A**
**(Multiple Choice Type Questions)**

1. Choose the correct alternative for the following: **10 × 1 = 10**

   (i) In comparison to conventional bulk MOSFETs, in SOI devices the body effect is
   (a) high (b) low
   (c) absent (d) same.

   (ii) In MOSFET devices the N-channel type is better than the P-channel type in which of the following respects?
   (a) It has better noise immunity
   (b) It is faster
   (c) It is TTL compatible
   (d) It has better drive capability.

   (iii) Increase in doping in substrate region of MOSFET will
   (a) decrease threshold voltage and increase substrate scattering
   (b) decrease threshold voltage and decrease substrate scattering
   (c) increase threshold voltage and decrease substrate scattering
   (d) increase threshold voltage and increase substrate scattering.

   (iv) The extremely high input impedance of a MOSFET is primarily due to
   (a) absence of its channel
   (b) negative gate-source voltage
   (c) depletion of current carriers
   (d) extremely small gate leakage current.

(v) The cut off frequency, $f_T$, of the MOSFET is

(a) proportional to transconductance($g_m$) and inversely proportional to total capacitance between gate to source/drain ($C_{gs}$+ $C_{gd}$).
(b) proportional to transconductance ($g_m$) and total capacitance between gate to source/drain ($C_{gs}$+ $C_{gd}$).
(c) inversely proportional to transconductance ($g_m$) and total capacitance between gate to source/drain ($C_{gs}$+ $C_{gd}$).
(d) inversely proportional to transconductance($g_m$) and total capacitance between gate to source/drain ($C_{gs}$+ $C_{gd}$).

(vi) Subthreshold swing of the MOSFET

(a) decreases with depletion capacitance and increases with oxide capacitance.
(b) decreases with depletion capacitance and decreases with oxide capacitance.
(c) increases with depletion capacitance and decreases with oxide capacitance.
(d) increases with depletion capacitance and increases with oxide capacitance.

(vii) In presence of volume inversion, the carrier mobility in thin film devices

(a)increases (b)decreases
(c) remains unchanged (d) none of these.

(viii) Hot electron effect causes

(a)oxide wear-out and breakdown
(b) change in threshold voltage
(c) finite gate current
(d) all the above.

(ix) $V_{dd}$ scaling

(a) makes the device slow.
(b) decreases the threshold voltage of the device.
(c) makes the device fast .
(d) increases the cut off frequency of the device.

(x) A FinFET with multiple fins of number N has an effective device width of

(a) $N(2\times H_{fin}+T_{fin})$ (b) $N(2\times H_{fin})+T_{fin}$
(c) $(2\times H_{fin}+T_{fin})$ (d) $(2\times H_{fin}+N\times T_{fin})$.





## Group - B

2. (a) Define threshold voltage. What do you mean by sub-threshold conduction?

(b) What is subthreshold swing? Why subthreshold swing is always higher than 60db/decade for a conventional MOSFET device?

**4 + (3 + 5) = 12**

3. (a) State the limitations of $SiO_2$ scaling. Explain how these may be overcome by the use of a high-K material as the gate dielectric.

(b) List the basic requirements of a high-K oxide. State some limitations of using high- K oxides.

**(2 + 4) + (4 + 2) = 12**

## Group - C

4. (a) Draw the small signal equivalent circuit of a MOSFET for high frequency analysis with the inclusion of non-quasi static effects.

(b) Derive the cut-off frequency ($f_T$) of conventional MOSFETs.

**6 + 6 = 12**

5. (a) How does substrate doping influence SCEs in MOSFETs? Why is the substrate chosen to be undoped for scaled DG-MOSFETs?

(b) Draw the cross-sectional diagram of a planar DG-MOSFET and explain how it is better compared to an FD-SOI device.

**(2 + 4) + 6 = 12**

## Group - D

6. (a) Explain how is FinFET a quasi-planar device?

(b) Discuss corner effects in Triple-Gate FinFETs. How can they be taken care of in these structures?

(c) What is Device-width quantization problem in FinFETs?

**4 + 4 + 4 = 12**

7. (a) Discuss the advantages of fully depleted SOI technology over partially-depleted SOI technology.