7. (a) Describe the working principle of binary-weighted resistor DAC implemented with R – 2R ladder network.

   (b) Evaluate the analog output voltage of the digital input word (1001) using serial charge redistribution DAC.

6 + 6 = 12

Group - E

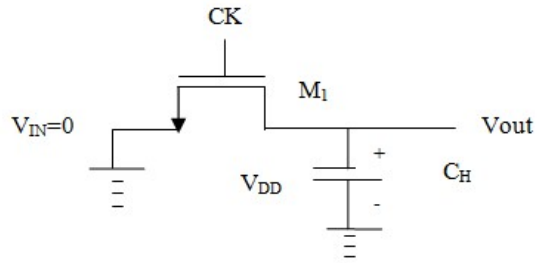
8. (a) Explain why a single common-source stage does not oscillate if it is placed in a unity gain loop? What is the requirement of the third inverting stage in a three-stage ring oscillator?

   (b) Calculate the oscillation frequency and minimum voltage gain per stage of a three-stage ring oscillator.

(2+6) + (4) = 12

9. (a) Discuss the necessity of switched capacitor circuits. Explain the track and hold operation of the sampling circuit implemented by a MOS device.

   (b) Calculate V_{out} as a function of time for the following circuit ignoring the channel length modulation effect.



(2+4) + (6) = 12

ANALOG IC DESIGN
(VLSI 5203)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

   (i) Linear amplification can be obtained from common – source MOSFET amplifier when biased in
   (a) saturation region (b) linear region
   (c) subthreshold conduction region (d) only exactly at $V_{DS} = V_{DS(sat)}$.

   (ii) The PSRR of the op-amp is given by
   (a) $PSRR = \frac{\Delta V_{DD}}{\Delta V_{out} A_V(S)}$ (b) $PSRR = \frac{A_V(S)\Delta V_{out}}{\Delta V_{DD}}$
   (c) $PSRR = \frac{\Delta V_{DD}}{\Delta V_{out}} A_V(S)$ (d) none of the above.

   (iii) The gate-to-channel capacitance of the MOSFET is given as
   (a) $C_{GC}=W_{eff}(L-LD)C_{ox}$ (b) $C_{GC}=W_{eff}(L-LD)C_{ox}$
   (c) $C_{GC}=W_{eff}(L+LD)C_{ox}$ (d) $C_{GC}=W_{eff}LC_{ox}$
   Where, LD stands for the lateral diffusion component.

   (iv) If the substrate terminals of the transistors forming the source – coupled pair of the CMOS differential amplifier is connected to their sources then
   (a) threshold voltages decrease
   (b) threshold voltages remain same
   (c) threshold voltages increase
   (d) threshold voltage depends on C_{bd} and C_{bs} .

(v) The performance of the switched capacitor circuits get influenced when the unity gain bandwidth of the op-amp becomes
(a) T=10/GB (b) T<10/GB (c) T>10/GB (d) T=1/GB.

(vi) Practical switched capacitor amplifier circuit utilizes
(a) series – parallel switched capacitor resistor emulation
(b) bilinear switched capacitor resistor emulation
(c) parallel switched capacitor resistor emulation
(d) series switched capacitor resistor emulation.

(vii) The dynamic range of a DAC can be expressed as
(a) 6.02 dB (b) – 6.02 dB
(c) 6.02N dB (d) – 6.02 N dB.

(viii) If the input signal contains no noise then
(a) $SNR_{in} = \infty$ and NF = 0 if the circuit does not have internal noise
(b) $SNR_{in} = \infty$ and NF = ∞ if the circuit does not have finite internal noise.
(c) $SNR_{in} = \infty$ and NF = 1 if the circuit has internal noise.
(d) $SNR_{in} = \infty$ and NF = ∞ even though the circuit may have finite internal noise.

(ix) If the line width of a spiral is doubled to reduce its resistance with D_{out}, *S*, and *N* remaining constant, the inductance
(a) reduces with decrease in diameter of the inner turns
(b) reduces with reduction in mutual coupling
(c) both (a) & (b)
(d) increases with increase in mutual coupling.

(x) The resolution of a digital-to-analog converter (DAC) is defined as
(a) the comparison between the actual output of the converter and its expected output.
(b) the deviation between the ideal straight-line output and the actual output of the converter.
(c) the smallest analog output change that can occur as a result of an increment in the digital input.
(d) its ability to resolve between forward and reverse steps when sequenced over its entire range.

Group - B

2. (a) Deduce the relationship between the drain current and the (W/L) ratios of the MOS transistor.

(b) Explain how V_{MIN} is reduced in the cascode current sink circuit.

6 + 6 = 12

3. (a) Explain the circuit operation of a CMOS differential amplifier using a current mirror load with the help of large signal analysis.

(b) Calculate the small-signal voltage gain of the push-pull amplifier. Also, illustrate graphically the voltage-transfer function of this amplifier.

6 + (4+2) = 12

Group - C

4. (a) Explain the phenomenon of intermodulation.
Suppose four Bluetooth users operate in a room. User 4 is in the receive mode and attempts to sense a weak signal transmitted by user 1 at 2.410 GHz. At the same time, users 2 and 3 transmit at 2.420 GHz and 2.430 GHz respectively. Explain what will happen.

(b) Briefly discuss "two-tone" test.
A Bluetooth receiver employs a LNA having a gain of 10 and an input impedance of 50 ohms. The LNA senses a desired signal level of -80 dBm at 2.410 GHz and two interferers of equal levels at 2.420 GHz and 2.430 GHz. For simplicity, assume LNA drives a 50 ohms load.
(i) Determine the value of α_3 that yields a P_{1dB} of -30 dBm.
(ii) If each interferer is 10 dB below P_{1dB}, determine the corruption experienced by the desired signal at the LNA output.

(4 + 2) + (2 + 4) = 12

5 (a) Analyse the parasitic capacitances of the spiral inductors using suitable model for this network.

(b) Can it be concluded that both the electric coupling and magnetic coupling to the substrate are eliminated if a grounded conductive plate is placed under the spiral inductor ? Explain the advantage and disadvantages of this approach.

8 + 4 = 12

Group - D

6. (a) Explain the role of sample and hold circuit in the ADC.

(b) Assume that the sampled analog input to a 4-bit pipeline algorithm ADC is 2 Volts. If V_{REF} = 5 Volts. Find the digital output word and the analog equivalent voltage. Show that if $V_{IN} = V_{REF}$, the ADC will have an error in the 5^{th} bit if the gain of the first stage is 1.875.

4 + (6 + 2) = 12