M.TECH/VLSI/2ND SEM/VLSI 5202/2018

VLSI DESIGN,VERIFICATION AND TESTING
(VLSI 5202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The output of physical design is
(a) layout (b) mask
(c) RTL (d) circuit design.

(ii) A MOS device can be used as a resistor in
(a) linear region (b) saturation region
(c) sub-threshold condition (d) mask region.

(iii) Memory with multiple read and write port is
(a) DRAM (b) ROM
(c) register file (d) SRAM.

(iv) Wire RC model acts as
(a) high pass filter (b) low pass filter
(c) band pass filter (d) all pass filter.

(v) Wafer test on an IC is performed during
(a) IC fabrication & manufacturing (b) IC application testing
(c) IC packaging (d) beta testing.

(vi) Transistor performs slowest at
(a) high voltage, high temperature
(b) high voltage, low temperature
(c) low voltage, high temperature
(d) low voltage, low temperature.

(vii) ATPG is based on
(a) Stuck at fault (b) BIST
(c) Bridging fault (d) DFT.

(viii) In a CMOS VLSI circuit the transistor fault detected by monitoring the power supply current during steady state is called
(a) stuck short transistor faults
(b) stuck Open transistor faults
(c) structural faults
(d) Behavioural faults.

(ix) Setup margin for a path is +10ps for cycle time of 200ps. If cycle time is reduced to 180ps, then new setup margin for the path will be
(a) +20ps (b) +10ps
(c) 0ps (d) -10ps.

(x) The critical path for a design refers to
(a) the path having maximum delay
(b) the path with minimum delay
(c) the path with optimum delay
(d) the path with no delay.

Group - B

2. (a) Explain the characteristic difference between the SRAM and DRAM with examples. Which applications prefer SRAM and which prefer DRAM?

(b) Design a combinational circuit using a 8×4 ROM. The circuit accepts a 3 bit number and generates an output binary number equal to the square of the input number

6 + 6 = 12

3. (a) Explain various components of a Memory Block with diagram.

(b) For a Memory Block of 32K memory locations and 32 data bits, explain how many row address bits and how many column address bits are needed.

6 + 6 = 12

Group - C

4. (a) In a CMOS inverter what are the lumped output load capacitance?

(b) What are propagation delays in an inverter? What is the average delay of an inverter?

6 + 6 = 12

5. (a) As per process technology, Metal-6 resistance is 10mohms/um and capacitance is 2ff/um. If 1mm wire is routed using Metal-6, draw circuit diagram of 3 segment pi model with appropriate resistance and capacitance value of individual segments.

(b) Why driver side of a wire needs to be of low resistance and receiver side of the wire needs to be of low capacitance, explain using Elmore Delay model

6 + 6 = 12

Group - D

6. (a) For a flip flop based sequential circuit, cycle time = 200ps, setup time = 25ps, clock-skew = 20ps, combinational delay = 60ps, clock to out delay of flop = 40ps. hold time = 40ps. What is setup margin and hold margin for the circuit?

(b) What is clock skew and what are the sources of clock skew?

6 + 6 = 12

7. (a) Explain H-Tree of clock distribution using circuit diagram.

(b) Draw positive edge triggered D Flip Flip using D Latch. Is Flip Flop Transparent designed like latch ?

6 + (4 + 2) = 12

Group - E

8. (a) For a given IC test, the number of detected faults is 1026 out of a Total number of faults of 1268, and rest are undetectable. Find fault coverage and the fault detection efficiency.

(b) Explain D-Algorithm with a circuit example.

6 + 6 = 12

9. (a) Consider a PC with 40 chips each having 90% fault coverage and 90% yield. Find the reject rate. What is a good way to reduce the reject rate?

(b) With a CMOS NOR gate explain with example how to detect transistor level stuck open and stuck short faults in the circuits.

6 + 6 = 12