(b) Draw the block diagram of ARM processor. What do you mean by course-grain parallelism?

(1 + 2 + 3) + (4 + 2) = 12

Group - E

8. (a) What are limitations of uniprocessor?

(b) How does a CMP (Chip Multi Processor) resolve those issues?

(c) Give examples of current applications with CMPs.

4 + 6 + 2 = 12

9. (a) Explain with the inter connection network architecture of NUMA and UMA.

(b) What is an SOC?

(c) What it typically consists of?

(d) What are basic design considerations of an SOC, and how is it fabricated?

4 + 2 + 2 + 4 = 12

VLSI PROCESSOR ARCHITECTURE
(VLSI 5201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) A computer process is a macro as it applies to an initial state and generates a
(a) program (b) data
(c) undefined state (d) final state.

(ii) Basic Computer Execution Cycle consists of
(a) Read, Write, Storage (b) Fetch, Decode, Execute
(c) Decode, Fetch, Store (d) Read, Fetch, Store.

(iii) Computers with R/M Architecture have instructions which can operate both on registers with one of the operands in
(a) register (b) temporary variable
(c) memory (d) board.

(iv) A Cycle is the time between state transitions in computers. If storage being reconfigured is registers we have a _____ _____
(a) memory cycle (b) machine cycle
(c) register cycle (d) computer cycle.

(v) A logic circuit in ALU is
(a) entirely combinational (b) entirely sequential
(c) both combinational and sequential (d) purely passive.

(vi) A _____ is a function that, when applied to a particular computer state, generates next state.
(a) filter (b) state
(c) command (d) program.

(vii) TMS320C5X DSPs are said to have advanced _____ architecture because they have _____ memory bus structures for program and data.
(a) Von Neumann, Same (b) Harvard, Alternate
(c) Von Neumann, Separate (d) Harvard, Separate.

(viii) The number of status registers in TMS3250C5X is
(a) 1 (b) 2 (c) 3 (d) 4.

(ix) A hardware accelerator is
(a) an active filter (b) not a co-processor
(c) same as a co-processor (d) a passive filter.

(x) Multi – core super scalar processor is a
(a) SISD (b) SIMD (c) MIMD (d) MISD.

Group - B

2. (a) Given a 32X8 ROM with an enable input, show the external connections necessary to construct 128x8 ROM with four chips and a decoder.

(b) Consider the following register transfer statements for two four bit registers R1 and R2

xT : R1 ← R1 + R2
x'T : R1 ← R1

Draw a hardware implementation of the two statements using two registers, a 4 bit adder, and a quadruple 2 to 1 line multiplexer.

6 + 6 = 12

3. (a) The Register transfer statement for a register R and the memory in a computer are as follows (The Xs are control function that occur at random):

X3'.X1:R ← M(AR)	Read Memory Word into R
X1'.X2: R ← ACC	Transfer ACC (accumulator) content to R
X1'.X3: M(AR) ← R	Write Content of R to a Memory Address.

The memory has data inputs, data outputs, address inputs and control inputs for READ and WRITE. Draw the hardware implementation of the memory and register R in block diagram form. Show how the control lines X1 to X3 are used to select the loading of Register R, select the inputs of the multiplexers that you include in the diagram, and determine the read write inputs for the memory.

(b) Show how a 9-bit micro-operation field in a micro-instruction can be divided into sub fields to specify 46 micro-operations. How many micro-operations can be specified in one micro-instruction?

8 + 4 = 12

Group - C

4. (a) Explain the different pipelining techniques.

(b) Design a floating point adder pipeline to add 100 floating point numbers.

(c) What are different types of pipeline hazards?

(d) The time delay for four segments in an arithmetic pipeline are as follows, t_1 = 50ns, t_2 = 30ns, t_3 = 95ns, and t_4 = 45ns. The interface registers delay is tr = 5ns.
(i) How long would it take to add 100 pairs of numbers in the pipeline?
(ii) How can we reduce the total time to about one-half of the time calculated in part (i).

2 + 3 + 2 + (2 + 3) = 12

5. (a) Distinguish between computer architecture and organization. Compare Harvard, Von Neumann and Modified Harvard Architecture and illustrate these architectures using block diagrams.

(b) Give the differences between CISC, RISC and VLIW architectures. Illustrate the instruction sets for CISC and RISC and VLIW with suitable examples.

(2 + 4) + 6 = 12

Group - D

6. (a) State Flynn's Classical taxonomy. Discuss the advantages and disadvantages of shared and distributed memory.

(b) Explain with suitable examples the parallelizable problem and the non-parallelizable problem.

6 + 6 = 12

7. (a) Define the ARM processor and give the special features of this processor. Explain the software interrupt, data processing, data transfer, swap, multiply, THUMB and branching instructions used in ARM processors.