DIGITAL VLSI DESIGN
(ECEN 3201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) According to Moore's Law, number of transistor per chip gets doubled in
(a) 16 Months (b) 18 Months
(c) 24 Months (d) 32 Months.

(ii) The fan-out of a digital circuit means
(a) amount of cooling required by the gate
(b) the number of other gates that can be connected to one of the gate's input
(c) the physical distance between the output pins of the circuit
(d) the number of other gates that can be connected to one of the gate's output

(iii) Value of "Lambda" in 180nm Process Node is
(a) 130nm (b) 65nm
(c) 90nm (d) 100nm.

(iv) BDD is used in
(a) high level synthesis (b) logic synthesis
(c) floorplan (d) routing.

(v) Minimum number of transistors in CMOS logic Y = AB + CD + EF is
(a) 10 (b) 12 (c) 14 (d) 16.

(vi) In Pseudo-nMOS logic, n transistor operates in
(a) cut-off region (b) saturation region
(c) resistive region (d) none of the above.

(vii) In VLSI Design which process deals with the determination of resistance and capacitance of interconnections?
(a) Floor planning (b) Placement and routing
(c) Testing (d) Extraction.

(viii) Which type of simulation mode is used to check the timing performance of a design?
(a) Behavioural (b) Switch-level
(c) Transistor-level (d) Gate-level.

(ix) In which of the following VLSI Methodology most manual effort is needed?
(a) FPGA (b) Gate Array
(c) Std Cell Based Semi Custom (d) Full Custom.

(x) The equivalent (W/L) of two nMOS transistors with (W_1/L) and (W_2/L) connected in parallel is
(a) $(W_1/L) + (W_2/L)$ (b) $(W_1/L) \times (W_2/L)$
(c) $[1/(W_1/L) + 1/(W_2/L)]^{-1}$ (d) $(W_1/L) / (W_2/L)$

Group – B

2. (a) What are differences between Full Custom Design and Std Cell based Semi Custom Design?

(b) Draw Circuit Diagram of 2 input XNOR gate using CMOS Logic.

(c) Draw Circuit Diagram of 2 input XNOR gate using CMOS Transmission Gate (TG).

4 + 4 + 4 = 12

3. (a) Design a CMOS gate for the logic function f(a, b, c) = Σm(0, 1, 3, 5, 6). Mention the widths of NMOS and PMOS for the above design so that the current driving capability remains same as that of the basic CMOS inverter.

(b) Draw a PLA circuit of the logic expression $f = X_1X_2 + X_1\overline{X_3} + \overline{X_1}\,\overline{X_2}X_3$

(c) Draw the output versus input voltage characteristics of a CMOS inverter when (i) $w_p = 2.5w_n$ (ii) $w_p = 8w_n$ (iii) $w_p = 0.6w_n$.

5 + 4 + 3 = 12

Group – C

4. (a) Design static CMOS circuit of the function $Y = \overline{A(D+E) + BC}$ and construct its layout using Euler Path Algorithm.

(b) Explain the operation of a 3-Transistor DRAM cell with the help of the circuit diagram.

7 + 5 = 12

5. (a) Draw Layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

   (b) What is the difference between "Micron Based Design Rule" and "Lambda Based Design Rule"?

   (c) Draw schematic and Stick Diagram of 2 input NAND gate.

4 + 3 + 5 = 12

Group – D

6. (a) Sketch a schematic of the circuit described by the following HDL code. Simplify to a minimum number of gates.

```
program1(input logic [3:0] a,
         output logic [1:0] y);
always_comb
  if  (a[0])       y = 2'b11;
  else if (a[1])   y = 2'b10;
  else if (a[2])   y = 2'b01;
  else if (a[3])   y = 2'b00;
  else             y = a[1:0];
endmodule
```

   (b) Implement the Data Flow Graph of the following function,
   x= a*b;
   y=a-c;
   z=x+d;
   x=x*c;
   Using Data Flow Graph, realize the data path logic.

6 + 6 = 12

7. (a) Write Verilog Description of a D-Flipflop.

   (b) Write Verilog Description of a 3 to 8 Decoder.

   (c) Write Verilog Description of 2:1 Mux.

4 + 4 + 4 = 12

Group – E

8. (a) Explain in detail the two kinds of transistor faults with the help of a CMOS NOR circuit and write the truth table to indicate the true and faulty outputs for different input combinations.

   (b) Explain D-Algorithm.

7 + 5 = 12

9. (a) Explain the principles of Built-In Self-Test (BIST). What are the advantages and disadvantages of BIST.

   (b) What are the 3 types of Delay Faults? Briefly state about the nature of these faults.

6 + 6 = 12