DIGITAL ELECTRONICS
(ECEN 2002)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Conversion of $(11011.101)_2$ to decimal number is
(a) 26.725 (b) 27.625
(c) 25.675 (d) 22.657.

(ii) A binary number with n bits all of which are 1 has the value
(a) $n^2 - 1$ (b) 2^n
(c) $2^{(n-1)}$ (d) $2^n - 1$.

(iii) To construct a K-map, the order is crucial and is obtained by using
(a) binary code progression (b) BCD code
(c) gray code progression (d) excess-3 code.

(iv) The OR operation can be produced with
(a) two NOR gates (b) three NAND gates
(c) four NAND gates (d) both answers (a) and (b).

(v) Excess-3 code is
(a) cyclic code (b) weighted code
(c) self-complementing code (d) error-correcting code.

(vi) If $(12x)_3 = (123)_x$, then the value of x is
(a) 2 (b) 4 (c) 5 (d) none of the above.

(vii) The fastest ADC is
(a) successive approximation (b) flash type
(c) dual slope (d) none of these.

(viii) An n-stage ripple counter can count up to
(a) 2^n (b) $2^n - 1$ (c) n (d) $2^{(n-1)}$.

(ix) The number of J-K flip-flops that is required to design a mod-11 asynchronous up counter is
(a) 3 (b) 4 (c) 5 (d) 6.

(x) A combinational circuit
(a) never contain memory element
(b) may sometimes contain memory element
(c) contain only memory element
(d) always contain memory element.

Group – B

2. (a) Simplify the Boolean function using tabulation method:
$F(A, B, C, D) = \sum m(0,2,3,6,7) + \sum d(8,10,11,15)$

(b) Design a 3 bit odd parity generator

7 + 5 = 12

3. (a) Minimize the Boolean function with K-map and realize using NAND gates only.
$F(A, B, C, D) = \sum m(2,3,8,10,11,12,14,15) + \sum d(0,1)$

(b) Represent
(i) $(4578)_{10}$ in Gray code
(ii) $(572.61)_8$ in common binary code.

7 + 5 = 12

Group – C

4. (a) Design a full substractor using half substractor module and necessary logic gates.

(b) Design a BCD to decimal decoder.

6 + 6= 12

5. (a) Realize 8:1 Multiplexer using 4:1 Multiplexer and necessary logic gates.

(b Implement a full substractor using
(i) decoder and necessary logic gates.
(ii) 4:1 Multiplexer.

6 + 6 = 12

Group – D

6. (a) Design an asynchronous counter that goes through the states 0-1-2-3-4-5-0.

(b) Realize J-K flip-flop using D flip-flop.

(c) Mention advantages of JK flip flop over SR flip flop.

6 + 4 + 2 = 12

7. (a) Design a synchronous MOD 3 UP/DOWN Counter using J-K flip-flops.

(b) A clocked sequential circuit has four states A, B, C and D as show in the state diagram of Fig.1. Assume state assignments as A=00, B=01, C=10 and D=11. Prepare the state table and draw circuit using D flip-flops.

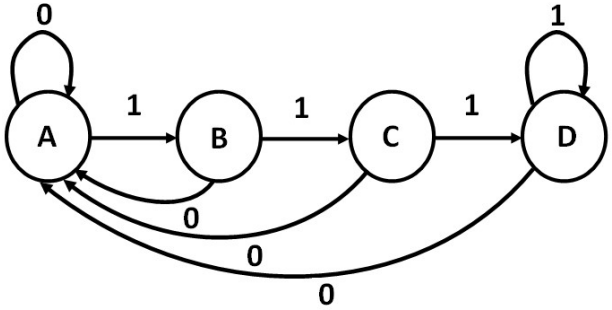

Fig. 1: State diagram of a clocked sequential circuit

6 + 6 = 12

Group – E

8. (a) Explain the operation of a Dual Slope ADC with the proper circuit diagram.

(b) What are the advantage of R-2R ladder type DAC over counter type DAC?

7 + 5 = 12

9. (a) Implement the function Y= (A+B)' using CMOS logic circuit.

(b) Draw a NOR Gate using RTL logic circuit.

(c) Draw the circuit of TTL NAND gate.

6 + 3 + 3 = 12