COMPUTER ORGANIZATION
(CSEN 2203)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Periodic refreshing is required for
(a) SRAM (b) DRAM (c) ROM (d) EPROM.

(ii) How many address bits are required for 1024 × 8 memory chip?
(a) 1024 (b)10 (c) 8 (d)12.

(iii) A system has 48 bit virtual address, 36-bit physical address. How many virtual pages and physical frames can the address space support ?
(a) 2^{36} , 2^{24} (b) 2^{12} , 2^{36} (c)2^{24} , 2^{34} (d) 2^{34} , 2^{36}.

(iv) How many RAM chips of size (256 K × 1 bit) are required to build 1MB memory?
(a) 8 (b) 10 (c) 24 (d) 32.

(v) Micro instructions are kept in
(a) cache memory (b) main memory
(c) control memory (d) none of these.

(vi) Address for the next executable instruction is stored in the
(a) stack pointer (b) program counter
(c) instruction register (d) none of these.

(vii) Booth's multiplication is used for
(a) multiplication of numbers in sign- magnitude form
(b) division of numbers in sign- magnitude form
(c) multiplication of numbers in 2's complement form
(d) division of numbers in 2's complement form

(viii) Cache memory
(a) increases performance (b) decreases performance
(c) increases machine cycle (d) none of these.

(ix) A decimal number has 10 digits. Approximately how many bits will the corresponding binary representation have?
(a) 30 (b) 50 (c)10 (d) 90

(x) Consider the following sequence of microoperations
MBR ← PC
MAR ← X
PC ← Y
Memory ← MBR
Which one of the following is a possible operation performed by the sequence?
(a) Instruction fetch (b) Operand fetch
(c) Conditional branch (d) Initiation of interrupt service.

Group – B

2. (a) Evaluate the arithmetic statement x=(A+B)/(C-D) in one two address machine instruction.

(b) What is instruction cycle?

(c) Registers R1 and R2 contain decimal values 1200 and 4600. What is the effective address of the memory operand and the type of addressing modes used in each of the following instructions?
(i) load 20(R1), R5
(ii) move #3000, R5
(iii) store R5, 30(R1,R2)
(iv) add –(R2) , R5
(v) sub (R1)+, R5

4 + 1 + 7= 12

3.(a) Explain with example the following addressing modes:
(i) Memory indirect, (ii) Relative,(iii) Immediate (iv) Register direct

(b) Differentiate between Von Neumann and Harvard architecture, explain using schematic diagram.

(c) What is Von Neumann bottleneck?

8 + 2 + 2 = 12

Group – C

4.(a) Explain with diagram, 4- bit carry look-ahead adder circuit.

(b) What is the gate delay for propagating carry in carry look-ahead adder?

(c) Use non restoring method to divide 10100011 by 1011.

4 + 2 + 6 = 12

5.(a) Give the merits and demerits of floating point and fixed point representations of storing real numbers.

(b) What is biased exponent? What are guard bits? Convert -32.75 to IEEE754 single precision floating point representation.

5 + 2 + 5 = 12

Group – D

6.(a) What are the advantages and disadvantages of micro-programmed control unit over hardwired control unit

(b) Find out the CPI in a multi-cycle CPU given the following:

Instruction Class	Number of clock cycles needed	% of each instruction class
Loads	5	22%
Stores	4	11%
Register-format instructions	4	49%
Branches	3	16%
Jumps	3	2%

(c) A processor has 28 distinct instruction with 13 instruction having 12 micro-instructions and 15 having 18 microinstructions. i) How many addresses are used in control memory? ii) If three instructions jump to another set of microinstructions each having 4 microinstructions then howmany addresses are now used in control memory? (Assume each microinstruction also stores a branch address)

6 + 4 + 2 = 12

7.(a) Explain the multiplication of two floating point numbers using pipeline.(Include diagram of various stages and buffers in between the stages).

(b) Explain structural hazard in pipeline (using diagram).Differentiate between RAW and WAR hazards.

6 + (3 + 3)= 12

Group – E

8.(a) Design a memory of size 1024X8 with the help of 4 RAM chips each of size 128 × 8 and ROM chip of size 512 × 8. Show the memory connection to CPU. Give the address range in hexadecimal for each RAM and ROM chip.

(b) Explain programmed I/O technique

. **9 + 3 = 12**

9.(a) Consider a 4 way set associative cache with 32 KB capacity and 512 byte blocks. The system generates 24 bit addresses.

i) How many blocks and sets does the cache have?
ii) How many address bits are required to find the byte offset within a cache block?
iii) How many bits are required to represent a tag field?

(b) Differentiate between the concept of memory mapped I/O and I/O mapped I/O.

(c) Explain DMA operation to transfer of block of data between memory and peripherals?

(3+ 2+2) + 2 + 3 = 12