B.TECH/AEIE/4TH SEM/AEIE 2201/2018
DIGITAL ELECTRONIC CIRCUITS
(AEIE 2201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The range of negative numbers for x-bit signed binary number system is
(a) -1 to $-(2^{n-1}-1)$ (b) 0 to -2^{n-1}
(c) -1 to $-2^{n}-1$ (d) 0 to $-2^{n}+1$.

(ii) Hexadecimal number corresponding to $(123.456)_8$ is
(a) 53.97 (b) 68.52 (c) 101.01 (d) 73.52.

(iii) A BCD adder requires
(a) two 4-bit adder (b) one 4-bit adder
(c) three 4-bit adder (d) none of the above.

(iv) Racing problem in a J-K flip-flop occurs at
(a) J=K=0 (b) J=1, K=0 (c) J=0, K=1 (d) J=K=1

(v) How many flip-flops are required to make a MOD-8 counter?
(a) 12 (b) 8 (c) 7 (d) 3.

(vi) Asynchronously connected two T flip-flops with T = 1 has a 4 kHz clock input. The Q output is
(a) a 5 kHz square wave (b) constantly HIGH
(c) a 1 kHz square wave (d) a 10 kHz square wave.

(vii) The logic function $A+\overline{ABC}$ is equivalent to
(a) A+BC (b) A+ABC
(c) $A+\overline{B}\,\overline{C}$ (d) $\overline{A}+\overline{B}\,\overline{C}$.

(viii) NOT gate can be realized by a 2- input EX-OR gate when
(a) both inputs are at logic 1 (b) one input is at logic 0
(c) one input is at logic 1 (d) both inputs are at logic 0.

(ix) In PLA design, we need
(a) fixed AND array and programmable OR array
(b) fixed AND and OR array
(c) programmable AND and OR array
(d) programmable AND array and fixed OR array.

(x) The logic circuit having LOWEST POWER DISSIPATION is _____.
(a) TTL (b) ECL (c) CMOS (d)DTL.

Group – B

2.(a) Write down the name of a universal gate and justify your answer.

(b) What is the difference between combinational and sequential circuit?

(c) Design a 3-bit Gray to binary code converter with necessary explanation.

4 + 2 + 6= 12

3.(a) Realize a 8:1 multiplexer by using 4:1 multiplexer.

(b) Minimize the logic function
$Y(A,B,C,D,E)=\sum m(0,1,2,3,8,9,16,17,20,21,24,25,28,29,30,31)$
using Karnaugh map.

4 + 8= 12

Group – C

4.(a) Design a common circuit to perform both addition and subtraction of 4-bit numbers.

(b) Design a D- flip flop with truth table by using S-R flip flop.

8 + 4 = 12

5.(a) Implement the logic function $Y(A,B,C,D) = \sum m(2,4,5,7,10,12,13,15,)$ using 8:1 multiplexer.

(b) Design a J-K flip flop with truth table by using only NAND gates.

8 + 4 = 12

Group – D

6. (a) Design a frequency divider circuit whose output frequency f_0 is divided by 32 of clock frequency.

(b) Design a synchronous 4-bit up-counter and explain with output waveforms.

6 + 6 = 12

7.(a) Design a 4-bit Johnson counter and explain its operation.

(b) Design a frequency divider circuit with output frequency 1/8-th of clock frequency.

6 + 6 = 12

Group – E

8.(a) Design a NAND gate using TTL technology.

(b) Write short notes on successive-approximation and flash type ADC.

5+7= 12

9.(a) Implement the given functions using programmable logic array (PLA)
$X(a, b, c, d)=\sum m(0, 2, 8, 10)$, $Y(a, b, c, d)=\sum m(1, 3, 9, 11)$.

(b) Write a short note on PROM device.

7+5 = 12