COMPUTER ORGANIZATION AND ARCHITECTURE
(MCAP 1205)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which of the following is lowest in memory hierarchy?
(a) RAM (b) Secondary memory
(c) Cache memory (d) Registers.

(ii) Cache memory acts between
(a) CPU and RAM (b) RAM and ROM
(c) CPU and Hard Disk (d) None of these.

(iii) A Stack-organised computer uses instruction of
(a) indirect addressing (b) two-addressing
(c) zero addressing (d) index addressing.

(iv) Von Neumann architecture is
(a) SISD (b) SIMD
(c) MIMD (d) MISD.

(v) Write Through technique is used in which memory for updating the data?
(a) Virtual memory (b) Main memory
(c) Auxiliary memory (d) Cache memory.

(vi) Status bit is also called
(a) binary bit (b) flag bit
(c) signed bit (d) unsigned bit.

(vii) In which addressing mode the operand is given in the instruction explicitly?
(a) Absolute (b) Immediate
(c) Indirect (d) Direct.

(viii) A group of bits that tell the computer to perform a specific operation is known as
(a) Instruction code (b) Micro-operation
(c) Accumulator (d) Register.

(ix) An instruction pipeline can be implemented by means of
(a) LIFO buffer (b) FIFO buffer
(c) stack (d) none of these.

(x) Data hazards occur when .....
(a) machine size is limited
(b) pipeline changes the order of read/write access to operands
(c) some functional unit is not fully pipelined
(d) none of the above.

Group - B

2. (a) Evaluate the following arithmetic statement using three addresses and two addresses instructions: X = (A+B)*(C+D)

(b) Differentiate between Hardwired control and Microprogrammed Control.

(c) Explain memory-reference instructions format.

4 + 4 + 4 = 12

3. (a) Describe how to convert decimal to IEEE 754 floating point representation and vice versa with suitable example.

(b) Differentiate between the Autoincrement and Autodecrement addressing mode.

8 + 4 = 12

Group - C

4. (a) Apply Booth's algorithm to multiply the two number $(-8)_{10}$ and $(2)_{10}$.

(b) Obtain the differences:
(i) $(8AB)_{16}$ - $(7CA)_{16}$
(ii) $(467)_8$ - $(764)_8$.

6 + (3 + 3) = 12

5. (a) Convert the following arithmetic expressions from infix to RPN
(i) A+B*[C*D+E*(F+G)]
(ii) A*B+A*(B*D+C*E).

(b) Write down the difference between restoring and non restoring division.

7 + 5 = 12

Group - D

6. (a) What do you mean by initialization of DMA controller? How DMA controller works? Explain with suitable block diagram.

(b) What is the advantage of cache memory?

8 + 4 = 12

7. (a) What is virtual memory? Explain the steps involved in virtual memory address translation.

(b) What is cache coherency and how is it eliminated?

(c) What is associative memory?

(2 + 4) + 4 + 2 = 12

Group – E

8. (a) What is the difference between serial and parallel transfer? Explain with proper example.

(b) What is Synchronous Bus Transfer? Explain with a timing diagram.

6 + 6 = 12

9. (a) Explain daisy chain priority.

(b) Define strobe control with an example.

(c) What are the different factors that can affect the performance of a pipelined system?

3 + 3 + 6 = 12