

M.TECH/ECE (VLSI)/1<sup>ST</sup> SEM/VLSI 5131/2017  
EMBEDDED SYSTEMS  
(VLSI 5131)

Time Allotted: 3 hrs

Full Marks: 70

*Figures out of the right margin indicate full marks.*

*Candidates are required to answer Group A and*

*Any 5 (five) from Group B to E, taking at least one from each group.*

*Candidates are required to give answer in their own words as far as practicable.*

**Group - A**

**(Multiple Choice Type Questions)**

1. Choose the correct alternative for the following: **10 × 1=10**

- (i) In a Real Time system *Time means that* the correctness of the system depends not only on logical results but also  
(a) on Random Output (b) the time the results are produced  
(c) on low Manufacturing Cost (d) on Power Consumption.
- (ii) A RTOS shall always have  
(a) time sensitive response (b) use of virtual memory  
(c) non-deterministic output (d) high interrupt latency.
- (iii) Property that does not characterize an embedded system is  
(a) random Output (b) real time output  
(c) low Manufacturing Cost (d) low Power Consumption.
- (iv) The logic family which takes the least power is  
(a) TTL (b) RTL  
(c) CMOS (d) ECL.
- (v) Which is not an embedded processor?  
(a) ARM 7 (b) ARM 9  
(c) AMD 29050 (d) IBM 370.
- (vi) The number of active elements in a DRAM cell is  
(a) 1 (b) 2  
(c) 6 (d) 9.
- (vii) The locality of reference justifies the use of  
(a) flash memory (b) cache memory  
(c) main memory (d) virtual memory.

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- (viii) A CAN device is a  
(a) serial and unidirectional (b) serial and bidirectional  
(c) parallel and unidirectional (d) parallel and bidirectional
- (ix) UART device  
(a) receives parallel data and stores as parallel  
(b) receives serial data and stores as serial  
(c) receives serial data and stores as parallel  
(d) receives parallel data and stores as serial
- (x) Watchdog timers enable an embedded system to  
(a) reduce overhead (b) restart in case of failure  
(c) reduce unit cost (d) improve efficiency

**Group - B**

2. (a) What are the common characteristics of an embedded system?  
(b) Which design metrics are optimized to meet the design challenges of an embedded system?  
(c) What are the major differences between a real time and non-real time system?  
(d) What is role of RTOS in embedded system? How does it differ from GPOS?

**3 + 3 + 3 + (2 + 1) = 12**

3. (a) Implement a full adder cell using a 3 × 8 decoder and OR gates.  
(b) Show the design of a synchronous decade up counter using JK Flip Flops. Modify the circuit to down count starting from 1111.

**4 + (5 + 3) = 12**

**Group - C**

4. (a) Explain the concepts of Watchdog timer and Reaction timer. Write the applications of both the timers.  
(b) What is "bouncing" in keypad? How does debouncing work?
5. (a) What is instruction pipelining?

**(4 + 3) + (2 + 3) = 12**

- (b) What are the pipeline hazards?
- (c) What are the major differences among Superscalar, Super pipelined, and VLIW approaches?
- (d) Let there be a 4 stage pipeline. The time it takes to process a sub operation in each stage is 20 ns. The pipeline executes 100 tasks in sequence. What is the speed up ratio?

$$3 + 3 + 3 + 3 = 12$$

**Group - D**

- 6. (a) Describe the addressing modes of 8051 microcontroller with proper examples.
- (b) Draw and explain the internal RAM structure of 8051 microcontroller.
- (c) Describe the Serial Control Register (SCON) of 8051 microcontroller.

$$5 + 4 + 3 = 12$$

- 7. (a) Explain briefly the ARM processor architecture memory organization with block schematic representation.
- (b) Explain the function of Distributed Interrupt Controller, for ARM11 MPCORE processors.
- (c) What is a Snoop Control Unit in ARM 11?

$$4 + 5 + 3 = 12$$

**Group - E**

- 8. (a) Why DMA based I/O is better than other I/O based technique?
- (b) What is the difference between isolated I/O and memory mapped I/O?
- (c) Explain DMA data transfer between memory and terminal peripheral.
- (d) What is the difference between vectored and non vectored interrupt?

$$3 + 3 + 4 + 2 = 12$$

- 9. (a) Distinguish between SRAM and DRAM. Explain their reading and writing operation.

- (b) What is cache mapping? Explain direct mapping for  $256 \times 8$  RAM and  $64 \times 8$  Cache memory.
- (c) An 8 bit DAC has a resolution of 15 mV/LSB. Determine:
  - (i) Full scale output voltage  $V_{fs}$ ?
  - (ii) Output voltage when the input digital word is "0001 0010".

$$4 + 4 + (2 + 2) = 12$$