M.TECH/ECE(VLSI)/1ST SEM/VLSI 5103/2017

MICROELECTRONICS TECHNOLOGY AND IC FABRICATION
(VLSI 5103)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Electronic grade silicon has a purity level of at least about
(a) 99% (b) 99.9999999%
(c) 99.9999% (d) 98%

(ii) Which of the following chemicals are used for anisotropic etching of SiO_2?
(a) HF and NH_4F (b) HNO_3, H_2O
(c) CH_3COOH, H_3PO_4 (d) KOH

(iii) Rapid thermal annealing is required after ion implantation to
(a) reduce the damage in the crystal due to nuclear energy loss
(b) reduce the damage in the crystal due to electronic energy loss
(c) increase the projected range
(d) decrease the lateral straggle.

(iv) The most common liquid source for boron is
(a) trimethyl borate (b) boron tribromide
(c) diborane (d) none of the above.

(v) Sputtering is a _____ process
(a) physical (b) chemical
(c) mechanical (d) none of the above.

(vi) Thermal oxidation of Silicon can be done by using
(a) wet oxidation (b) dry oxidation
(c) both (a) and (b) (d) none of the above.

(vii) The liquid source employed for basic diffusion of Phosphorous in Silicon is
(a) P_2O_5 (b) PH_3 (c) $POCl_3$ (d) PH_4.

(viii) For immersion etching, the wafer is immersed in the etch solution and _____ agitation is required to ensure etch uniformity and consistent etch rate.
(a) electrical (b) mechnaical
(c) thermal (d) nuclear.

(ix) Metallization is used for
(a) interconnection (b) packaging
(c) protection (d) all the above.

(x) A plasma has _____ numbers of positive and negative charges.
(a) equal (b) may be equal
(c) unequal (d) may be unequal.

Group – B

2. (a) Mention the uses of SiO_2 in the Semiconductor fabrication industry.

(b) Prove that if a SiO_2 layer is grown by thermal oxidation, the thickness of Si consumed is 0.44 times the thickness of SiO_2. Given, the molecular weight of Si is 28.9 g/mol and the density of Si is 2.33 g/cm^3. The corresponding values for SiO_2 are 60.08 g/mol and 2.21 g/cm^3.
4 + 8 = 12

3. (a) Differentiate between dry and wet oxidation.

(b) Discuss the kinetics of oxidation. Derive from first principles, an expression for the oxide thickness in terms of the oxidizing time, diffusion coefficient of the oxidizing species and the concentrations.

(c) Write a short note on dopant redistribution during oxidation.
3 + (2 + 3) + 4 = 12

Group – C

4. (a) Discuss how impurity doping can be carried out in the semiconductor by using diffusion and ion implantation process. Explain the mechanism of vacancy diffusion and interstitial diffusion in semiconductors.

(b) Discuss Fick's law of diffusion and draw the doping profiles for constant source diffusion.
6 + 6 = 12

5. (a) Discuss the advantages of doping using ion implantation method over the diffusion method.

(b) Draw a schematic diagram of an ion-implantation system and explain its basic principle of operation.

4 + 8 = 12

Group – D

6. (a) What is a positive photoresist?

   (b) Explain with suitable diagrams the steps of pattern transfer using a positive photoresist.

2 + 10 = 12

7. (a) What is wet chemical etching? What are the characteristics of an ideal etchant used for wet chemical etching?

   (b) Discuss Buffered Oxide Etching, its advantages and limitations.

6 + 6 = 12

Group – E

8. (a) State the principal limitations of conventional lithography. How are these overcome in electron-beam lithography?

   (b) Write short notes on the following:
   (i) Reactive Ion Etch
   (ii) Multi-level metallization

(2 + 2) + (2 × 4) = 12

9. (a) Explain with suitable diagrams the process steps of fabrication of an n-channel MOSFET.

   (b) Compare MOSFET and MESFET technologies.

7 + 5 = 12