M.TECH/ECE(VLSI)/1ST SEM/VLSI 5102/2017

DIGITAL IC DESIGN
(VLSI 5102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Value of "Lambda" in 0.5 μm Technology is
(a) 0.25 μm (b) 0.5 μm
(c) 1 μm (d) 2 μm.

(ii) According to Moore's Law, Number of Transistor per chip gets doubled in
(a) 12 Months (b) 18 Months
(c) 24 Months (d) 30 Months.

(iii) Pentium 4 chip belongs to below category
(a) VLSI (b) LSI (c) ULSI (d) GSI.

(iv) Most popular interconnect material is
(a) Gold (b) Silver
(c) Aluminium (d) Silicon Dioxide.

(v) For a Standard Cell Layout
(a) height is fixed (b) width is fixed
(c) both height and width are fixed (d) none of the above.

(vi) Memory Design is normally done using _____ Method
(a) Full Custom (b) Std Cell based Semi Custom
(c) FPGA (d) Gate Array.

(vii) BDD is used in
(a) High Level Synthesis (b) Logic Synthesis
(c) Floorplan (d) Routing.

(viii) Minimum Number of Transistors in CMOS logic Y = AB + CD + EF is
(a) 10 (b) 12 (c) 14 (d) 8.

(ix) KL Algorithm is related to
(a) Routing (b) Partitioning
(c) Logic Synthesis (d) High Level Synthesis.

(x) 0.7 Technology Scaling enables Layout area scaling of
(a) 0.7 (b) 0.5 (c) 0.4 (d) 0.6.

Group – B

2. (a) Draw Circuit Diagram of a D-Latch using CMOS Transmission Gate (TG).

(b) Draw Circuit Diagram of a Negative Edge Triggered D-Flip Flop using D-Latch.

(c) Draw Circuit Diagram of 2 input XNOR gate using CMOS Logic.

(d) Draw Circuit Diagram of 2 input XOR gate using CMOS Transmission Gate (TG).

3 + 3 + 3 + 3 = 12

3. (a) What are various Capacitance Components of a MOS Transistor?

(b) Draw VTC (Voltage Transfer Curve) of CMOS Inverter. How VTC of CMOS inverter will change if Width of PMOS is increased?

(c) For a CMOS Inverter V_{OH} = 5 V, V_{OL} = 0 V, V_{IH} = 3.4 V, V_{IL}= 2.2 V. What is the value of NM_H and NM_L?

4 + (3 + 3) + 2 = 12

Group – C

4. (a) What are differences between Full Custom Design and Std Cell based Semi Custom Design?

(b) Explain Euler Path solution of a CMOS gate which represents function f = (AB+C+D) ! (! Means Bar).

(c) Draw Stick Diagram of the same CMOS gate based on Euler Path Solution.

4 + 3 + 5 = 12

5. (a) Draw Y Chart for VLSI Design.

(b) Draw Domino Implementation of 3 input NOR gate

(c) Implement f = A.B Boolean logic using Transmission Gate.

3 + 4 + 5 = 12

Group – D

6. (a) Describe difference between Behavioral and Structural model of VHDL coding using an example. Write VHDL Behavioral model for a D–Flip Flop.

   (b) Write VHDL model for a full adder circuit using structural model.

(4 + 3) + 5 = 12

7. (a) Explain high level synthesis flow.

   (b) Explain control and data flow graph with an example.

   (c) Explain ASAP and ALAP algorithm of scheduling.

4 + 4 + 4 = 12

Group – E

8. (a) Draw the flow diagram of Physical Layout Automation. Draw the flow diagram of Logic Synthesis.

   (b) Draw the BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a $\leq$ b $\leq$ c. Create ROBDD Diagram and obtain the corresponding optimized Boolean expression.

(3 + 3) + (3 + 3) = 12

9. (a) For Floor planning problem, what are inputs, outputs and Objective (Cost) function?

   (b) Write problem formulation of Global Routing using Steiner Tree.

   (c) Explain Maze Routing.

3 + 4 + 5 = 12