M.TECH/ECE (VLSI)/1ST SEM/VLSI 5101/2017
VLSI DEVICE & MODELLING
(VLSI 5101)

Time Allotted: 3 hrs **Full Marks: 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and
Any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1=10**

(i) The energy band gap of GaAs is
(a)1.12 ev (b) 0.72 ev (c) 1.43 ev (d) 1.44 ev.

(ii) The contact potential of a pn-junction is dependent on
(a) Intrinsic carrier concentration (b) doping concentration
(c) absolute temperature (d) all of the above.

(iii) ITRS is the abbreviation of
(a) International Technology Roadmap for Semiconductor Devices
(b) International Technology Roadmap for Semiconductors
(c) Innovative Technology Reigning for Semiconductor Devices
(d) None of these.

(iv) Which MOSFET allows the flow of drain current even with zero gate to source voltage just due to existence of channel between drain and source terminals?
(a) Depletion MOSFET (b) Enhancement MOSFET
(c) Depletion-Enhancement MOSFET (d) All of the above.

(v) In a MOSFET channel with strong inversion, the dominant current component is due to
(a) drift
(b) diffusion
(c) drift and diffusion both
(d) leakage current of drain source p-n junctions.

(vi) At room temperature a semiconductor material behaves like a
(a) perfect insulator (b) conductor
(c) slightly conducting (d) none of the these.

(vii) The process of adding impurities to a pure semiconductor is called
(a) Mixing (b) Doping
(c) Diffusing (d) none of the these.

(viii) EKV drain current model describes the device operation for
(a) Weak inversion (b) Strong inversion
(c) Moderate inversion (d) all the three regions of inversion.

(ix) Velocity saturation in a short channel device causes the drain current to saturate at
(a) same Vds (b) lower Vds
(c) Higher Vds (d) Vt.

(x) The Ebers-Moll model for a transistor describes it as two _____ in series
(a) diodes (b) resistors
(c) capacitors (d) inductors.

Group – B

2. (a) Compare homojunction and heterojunction using schematic diagram.

(b) What are the different types of heterojunction structures?

(c) What do you mean by Ballistic Transport?

4 + 4 + 4 = 12

3. (a) Differentiate between lateral and vertical transistors.

(b) Draw the equivalent circuit representation of the basic DC Ebers-Moll model of an n-p-n transistor and express the emitter and collector currents in terms of the applied voltages.

2 + 10 = 12

Group – C

4. (a) Draw the schematic cross section of n MOS capacitor and its energy band diagram under different bias conditions.

(b) Explain subthreshold swing. Why subthreshold swing cannot be below 60mV/decade for a MOS transistor? How can it be improved?

6 + (2 + 2 + 2) = 12

5. (a) Draw the output characteristics of an nMOS and write down the expressions for the current flowing through the device in its different regions of operation.

(b) Draw and explain the capacitance-voltage characteristics of a MOSFET.

6 + 6 = 12

Group – D

6. (a) What are short-channel MOSFETs? Discuss the threshold voltage roll-off, channel length modulation and the DIBL phenomenon in short channel MOSFETs.

(b) Write a short note on ITRS.

(1 + 6) + 5 = 12

7. (a) What are the advantages of a fully depleted MOSFET over the partially depleted MOSFET structure?

(b) Is the overlap of the gate with the source and drain regions required, beneficial or irrelevant? Explain its effects.

6 + 6 =12

Group – E

8. (a) How can the SPICE LEVEL 1 MOSFET model be developed from the expression of the drain current?

(b) Discuss the accuracy and limitations of the LEVEL 1 MOSFET model and how it can be improved by LEVEL 2 MOSFET model.

6 + 6 = 12

9. (a) What are compact MOSFET models? Why the development of compact model is necessary for usage in circuit simulators?

(b) Compare the threshold voltage-based, charge-based and surface-potential-based compact models for a MOS transistor.

(3 + 3) + 6 = 12