## MCA /1<sup>st</sup> SEM/MCAP 1101/2017

## DIGITAL LOGIC DESIGN (MCAP 1101)

Time Allotted: 3 hrs

Full Marks: 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and

Any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

# Group – A (Multiple Choice Type Questions)

- 1. Choose the correct alternative for the following: **10** × **1**= **10** 
  - (i) An OR gate has 6 inputs. The number of input words in it's truth table are (a) 6 (b) 32 (c) 64 (d)128.
  - (ii) The simplification of the Boolean expression (A'BC')' + (AB'C)' is (a) 0 (b) 1 (c) A (d) BC.
  - (iii) Find out the unknown base x when  $(123)_8 = (313)_x$ . (a) 6 (b) 5 (c) 7 (d) 4.
  - (iv) What is the Grey code for the binary number  $(01001)_2$ ? (a) 01101 (b) 010101 (c) 101010 (d) none of these.
  - (v) The number of control lines for a 8 to 1 multiplexer is (a) 2 (b) 3 (c) 4 (d) 5.
  - (vi) One disadvantage of R-S flip-flop is,
    (a) it has only single output
    (b) it has no enable input
    (c) it has RACE condition
    (d) it has no clock input.
  - (vii) The Octal equivalent of  $(386)_{10}$  is (a) 606 (b) 602 (c) 620 (d) 622.
  - (viii) Maximum no of inputs connected to gate is called
    (a) fan
    (b) fan in
    (c) fan out
    (d) out come.

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(ix)	2's complement representation of 1101 0110 is	
	(a) 0001 1001	(b) 00101010
	(c) 1010 1001	(d) none.

- (x) A Boolean expression  $\Sigma(1,3,6,7)$  is equivalent to (a)  $\Pi(0,2,4,5)$  (b)  $\Pi(0,1,4,5)$ (c)  $\Pi(0,2,4,6)$  (d)  $\Pi(1,2,3,5)$ . **Group - B**
- 2. (a) Perform the arithmetic operations (+42) + (-13) and (-42) (-13) in binary signed 2's complement representation.
  - (b) Add the following numbers using BCD number system (37) + (15). Convert the following hexadecimal-number (13AC45.B3D)<sub>16</sub> into it's octal equivalent.

(3+3) + (3+3) = 12

- 3. (a) Convert the Grey-code 1110111010101 into it's equivalent Binary Code.
  - (b) Perform the following subtraction of two unsigned numbers using 1's complement: 11001 - 10110
  - (c) Draw the block diagram of BCD adder and explain how it works.
  - (d) Convert the octal number 7401 to its Binary equivalent.

3 + 3 + 3 + 3 = 12

## Group – C

- 4. (a) What are universal gates? Construct a logic circuit using NAND gates only for the expression X = A. (B + C)
  - (b) Convert the following Boolean-function into product of sum(POS) form:

 $F(w, x, y, z) = \Sigma(2, 3, 10, 11, 12, 13, 14, 15).$ 

(2+4)+6=12

5. (a) Simplify the following Boolean-function using K-map method and draw the circuit diagram using minimum number of NAND gates.  $F(w, x, y, z)=\Sigma(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14).$ 

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 (b) Reduce the following Boolean expression into five literals: ABC + A'B'C + A'BC + ABC' + A'B'C' .
 (where X' implies the complement of X)

Group - D

6. (a) Implement the following function using 4-to-1 multiplexer.  $\sum_{i=1}^{n} \sum_{j=1}^{n} \sum_{i=1}^{n} \sum_{j=1}^{n} \sum_{j=1}^{n} \sum_{i=1}^{n} \sum_{j=1}^{n} \sum_{j=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n$ 

$$F(A, B, C) = \sum_{i=1}^{n} (2, 3, 5, 6)$$

(b) Implement a full-adder circuit with a Decoder and two OR gates.

6 + 6 = 12

- 7. (a) How many 128 × 8 memory chips are needed to provide a memory capacity of 4096 × 16? Also indicate the size of address bus and data bus for 4096 × 16 bits memory.
  - (b) Draw the logic diagram of a full subtractor using half subtractors and explain its working with the help of a truth table.
  - (c) What are the two approaches to reduce the delay in the adders?
     (1 + 1 + 1) + 6 + 3 = 12

## Group – E

- 8. (a) What is the difference between a latch and a flip-flop?
  - (b) Construct a shift register from S-R flip-flops. Explain its working.
  - (c) Distinguish between synchronous sequential circuit and asynchronous sequential circuit.

2 + (2 + 2) + 3 = 12

- 9. (a) What is a shift register? Can a shift register be used as a counter? If yes, explain how?
  - (b) What is race around condition in flip-flop?
  - (c) Justify with diagram that ,T flip-flop is a single input version of JK flip.
     (2 + 4) + 3 + 3 = 12