I plane polarized electron

raphically the variation of

ave.

evelop the analogy betwee ansmission line.

lossless transmission line 0 MHz. The line paramet the characteristic impe locity.

ing Biot-Savart law, deri a long co-axial cable with a) respectively.

ve that  $\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}$ 

te Lorentz force equation aight conductor of lengt

e and explain Maxwell's inguish between transfo

ve the wave equation fo t is polarization of elect

#### B.TECH/EE/3rd SEM /ELEC 2101/2015 2015

#### **Analog & Digital Electronics** (ELEC 2101)

Allotted: 3 hrs

Full Marks: 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and ou 5 (five) from Group B to E, taking at least one from each group.

ates are required to give answer in their own words as far as practicable. Group - A

(Multiple Choice Type Questions)

10 x 1=10 the correct alternatives for the following:

output impedance of a series voltage amplifier is (a) Ro (1+AB).

(b)  $R_0/(1+A\beta)$ .

(c)  $\beta R_0 / (1+A)$ .

(d) none of these.

astable multivibrator generates

(a) triangular waveform.

(b) sinusoidal waveform.

(c) square waveform.

(d) none of these.

he output impedance of an Op-amp should be

(a) as small as possible.

(b) close to unity.

(c) close to zero.

(d) as large as possible.

ideal regulated power supply should have regulation equal to

(a) maximum.

(b) zero.

(c) 75%.

(d) 50%.

avoid false triggering of the NE555 timer, the RESET pin is generally connected to

(a) +Vcc.

(b) -Vcc.

(c) Ground.

(d) No connection.

JR gate can be expressed as a gate

- (a) producing output "1" when any one of its input is "0" else "0".
- (b) producing output "0" when any one of its input is "1" else "1".
- (c) producing output "1" when any one of its input is "1" else "0".
- (d) producing output "0" when any one of its input is "0" else "1".

Vhich expression is valid for NAND gate?

(a) NAND gate is equivalent to input inverted AND gate.

(b) Output inverted OR gate.

(c) Input inverted OR gate.

(d) None of the above.

2101

Answer any three que

ELECTOR ODD

Two point charges C nd (2, 0, 5) m r ermeability 2.5. Find circular disc of radi the origin. Charge int (0, 0, h).

plane polarized el phically the variation

elop the analogy b smission line. ssless transmission

MHz. The line par ne characteristic ity.

Biot-Savart law. ong co-axial cable respectively.

that  $\nabla \times \vec{H} = \vec{J} +$ 

Lorentz force equ ht conductor of l

d explain Maxw ish between tran

ne wave equation polarization of el

### B.TECH/EE/3rd SEM /ELEC 2101/2015

- (viii) To reduce logical expression, Karnaugh Map (K-Map) is preferable using Boolean rules because
  - (a) K-Map does not require the rules to remember.
  - (b) K-Map reduces the variable for adjacency.
  - (c) both (a) and (b).
- (d) none of the above.
- (ix) To express a large number more number of digits are required for
  - (a) Hexadecimal system
- (b) Decimal system

(c) Binary system

- (d) Octal system.
- (x) Synchronous counter is preferable to ripple counter because
  - (a) Synchronous counter clocks each stage simultaneously.
  - (b) Design of ripple counter is complicated.
  - (c) Synchronous counter receives clocks of higher frequencies as input
  - (d) None of the above.

#### Group - B

2.(a) Realize the following linear differential equation using Op-amp

$$\frac{d^3y}{dt^3} + 4\frac{d^2y}{dt^2} + 3\frac{dy}{dt} + 5y = 20$$

- (b) In connection to the specifications of an Op-amp, explain the terms:
  - i) supply voltage rejection ratio
  - ii) offset voltage adjustment range.
- (c) Explain the principle of operation of a differential amplifier using BITs.

- 3.(a) Deduce the expressions of closed loop voltage gain for a
  - i) voltage series feedback amplifier.
  - ii) voltage shunt feedback amplifier.
- (b) Design a practical integrator circuit to properly process input sinusoida95 154). from 10Hz to 1 kHz. The input amplitude is 10mV. Draw the complete component values. Positive and negative saturation output voltages of th 12V and -12V respectively.
- (c) Discuss about the problems in a basic differentiator circuit. How do we over (3+3)

#### Group - C

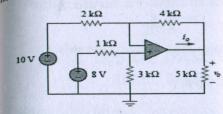
diagram. Derive the expression of the frequency of oscillation.

## 6/3" SEM /ELEC 2101/2015

schmitt trigger circuit has the following specifications:

 $_{100\Omega}$ ,  $R_2$  =  $56k\Omega$  , input voltage = 1V p-p sine wave, Op-amp is type 741 with voltages = ± 15V. Determine the threshold voltages and draw the output (For 741 the maximum output voltage swing is ± 14V)

an we regulate the amplitude of the output voltage in a Schmitt trigger circuit? the output voltage of the circuit given below:



5 + 4 + 3 = 12

/2015

TH

as fo

the

the help of a block diagram explain the principle of operation of one-shot hyibrator using

- Op-amp
- ii) 555 timer

the output voltage waveform and derive the expression for time period.

ing 7805C voltage regulator design a current source that will deliver 0.25A current 18Ω, 10W load.

(5+5) + (2) = 12

#### Group - D

nd the 9's complement and 10's complement for the following numbers: 7, 14, 83.

btract using 9's complement and 10's complement method: (13 - 7), (54 - 21),

btract using 1's complement and 2's complement method: (11012 - 01112),  $)110_2 - 11011_2).$ 

nvert the following binary to Gray code: 10112, 101012.

3+3+4+2=12

te De Morgan's Theorems and realise in circuit.

4. (a) Explain the working principle of a Hartley's oscillator with the help of a way the equivalent OR gate using NAND gates and equivalent AND gates using NOR

**ELEC 2101** 

2

01

3

nswer any three qu vo point charges ( d (2, 0, 5) m meability 2.5. Fir circular disc of rac he origin. Charge nt (0, 0, h).

> lane polarized hically the varia

op the analog nission line. sless transmis Hz. The line characterist

> Biot-Savart g co-axial spectively.

at  $\nabla \times \vec{H} =$ 

rentz forc conducto

> explain 1 h betwee

> > wave e larizatio

i) Write the truth table and transfer it into Karnaugh Map. ii) Write the minimum SOP expression and realise the circuit.

(d) Design a 2 line to 4 line decoder.

2+2+(2+

#### Group - E

- 8.(a) Design SR flip-flop using NAND gates and NOR gates separately.
  - (b) Design J-K flip-flop from basic SR flip-flop.
- (c) Draw the diagram for Master-Slave J-K flip-flop. State the operation briefly
- (d) Design a 4-bit ripple binary counter. Briefly explain its operation.
- 9.(a) Draw the circuit diagram for 4 bit R-2R ladder DAC.
  - (b) Explain the operation of TTL circuit.
- (d) Explain the dual slope ADC with diagram.

# B.Tech/ECE/EE/3rd Sem/ELEC-2102/2015

## 2015

CIRCUIT THEORY (ELEC 2102)

TE

ce

Alloted: 3 Hours of the base of the Full Marks: 70 Figures out of the right margin indicate full marks.

andidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group. andidates are required to give answer in their own words as far as practicable

# GROUP - A

(Multiple Choice Type Questions)

Choose the correct alternatives for the following: [10×1=10]

- Laplace transform of delayed unit impulse function  $\delta(t-1)$  is
  - (a) 1

(b) e-s

(c) 0

- (d) s
- When two inductive coils having self-inductance L<sub>1</sub>,L<sub>2</sub> and mutual inductance M in between them are connected in series aiding, the equivalent inductance across the series combination will be
  - (a)  $L_1 + L_2 + 2M$  (b)  $L_1 + L_2 2M$
  - (c)  $L_1 + L_2 + M$  (d)  $L_1 + L_2 M$

EC 2102

[Turn over]