(viii) Switched Capacitor Circuit Realizes
(a) capacitance (b) resistance
(c) inductance (d) current Source.

(ix) DIBL can be mitigated by
(a) making the junction depth shallow
(b) increasing the doping concentration
(c) both (a) and (b)
(d) none of the above.

(x) The performance of a current mirror circuit depends on
(a) V_{th} (b) aspect ratio
(c) channel length modulation (d) all of the above.

Group – B

2. (a) Derive the drain current equation of a PMOS (E-type). Design a 2mA current source using following parameter: k_n=150μA/V², $V_{th,n}$= 0.46V and W/L=3/0.65.

(b) What do you mean by scaling of a MOSFET? Describe different type of scaling that can be applied in VLSI device design.

(5 + 3) + 4 = 12

3. (a) Explain the accumulation, depletion, and inversion condition of a MOS capacitor. Assume the semiconducting material is a p-type material.

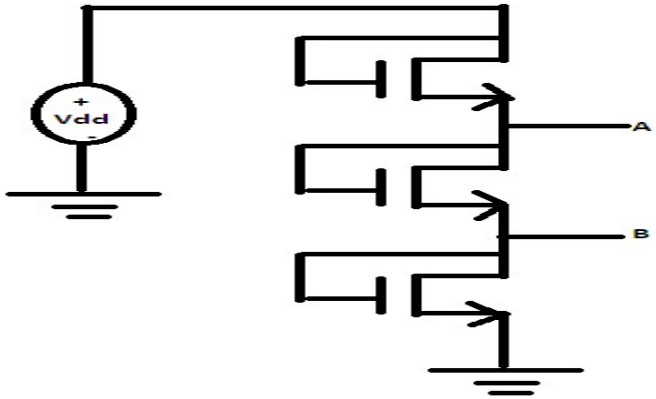
(b) Derive the threshold voltage expression of the above said MOS capacitor. What is the effect of substrate bias on threshold voltage of a MOSFET? Show with proper expression.

6 + (3 + 3) = 12

Group – C

4. (a) Draw a complete the small signal equivalent model of a NMOS. Describe and derive the expressions of each component of it. Find the small signal equivalent model of the NMOS when change in i_D is 2μA and V_{GS} is 0.3V. Assume the MOSFET is having the following parameters: β=95 μA/V², V_{GS} =0.5V, $V_{th,n}$ =0.2V, V_{DS} =1V and V_{BS} =0V.

(b) Design the following voltage divider circuit to produce $V_{dd}/3$ at node A and $V_{dd}/4$ at node B.



(6 + 3) + 3

5. (a) Explain CMOS Fabrication flow step by step using self aligned N Process Techniques.

(b) Draw Structure of SOI and FINFET Transistor.

8 + 4

Group – D

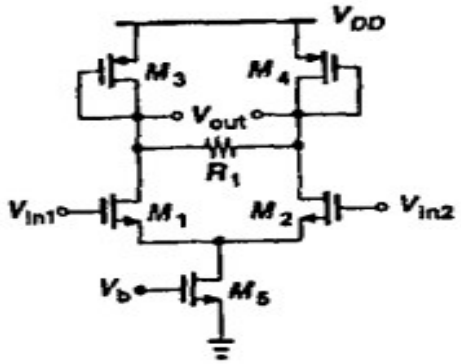
6. (a) What are design Steps for Analog VLSI Flow?

(b) Draw Large Signal Models for NMOS.

(c) What is Transconductance and on what parameters does it dep

3 + 4 + 5

7. (a)



Give the differential gain and output impedance expression above shown circuit.

(b) Why do we require compensesation in CMOS OPAMP circuit.

(c) Explain about CMOS sample and Hold circuit with neat waveforms.

6 + 3 + 3 = 12

Group – E

8. (a) Explain Basic Current Mirror Circuit.

(b) What is advantage of using cascode Current Mirror?

(c) Explain CMOS bandgap reference circuits.

3 + 4 + 5 = 12

9. (a) What is λ-based design? What are its merits and demerits?

(b) What is twin tub process?

(c) Differentiate between dry and wet oxidation. Write down the corresponding chemical equations.

(d) What is chemical etching?

4 + 2 + (1 + 2) + 3 = 12

MICROELECTRONICS & ANALOG VLSI DESIGN
(ECEN 3103)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) According to Moore's Law, Number of Transistor per chip gets doubled in
(a) 16 Months (b) 18 Months (c) 24 Months (d) 30 Months.

(ii) If it is required to reduce both the output impedance and the input impedance of an amplifier, what type of feedback will you use?
(a) Negative (b) Positive
(c) Negative followed by positive (d) Positive followed by negative.

(iii) Value of "Lambda" in 130nm Process Node is
(a) 130nm (b) 65nm (c) 90nm (d) 100nm.

(iv) Saturation Region of Ideal MOS Transistor can be modelled as
(a) resistance (b) capacitance
(c) current Source (d) voltage Source.

(v) Photoresist is a _____ compound.
(a) radiation-sensitive (b) radiation-insensitive
(c) radiative (d) non-radiative.

(vi) 3D Transistor is created using which of the following Fabrication Process?
(a) SOI (b) Planner
(c) FINFET (d) None of above.

(vii) The threshold voltage _____ voltage in SCE
(a) shifts towards lower (b) shifts towards higher
(b) remains same (d) none of the above.