VSLI DESIGN AUTOMATION
(ECEN 4181)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

   (i) Value of "Lambda" in 0.5 μm Technology is
   (a) 0.25 μm (b) 0.5 μm (c) 1 μm (d) 2 μm.

   (ii) Output of physical design is
   (a) circuit (b) layout
   (c) logical model (d) RTL Schematic.

   (iii) Left Edge Algorithm is used for
   (a) Floor planning (b) Placement
   (c) Routing (d) Partitioning.

   (iv) Ideal Current Source has Resistance of value
   (a) 0 Ω (b) Infinite
   (c) 100 K Ω (d) 10 Ω.

   (v) Kernighan – Lin algorithm is used for
   (a) Partitioning (b) Placement
   (c) Floor planning (d) Routing.

   (vi) For a Standard Cell Layout
   (a) height is fixed (b) width is fixed
   (c) both height and width are fixed (d) none of the above.

   (vii) With decrease of V_{dd}, the Delay of a CMOS inverter
   (a) increases (b) decreases
   (c) remains same (d) becomes infinite.

   (viii) Minimum Number of Transistors in CMOS logic Y = ABC + DE is
   (a) 12 (b) 6 (c) 14 (d) 10.

   (ix) Scaling is done for
   (a) improving the switching speed
   (b) decreasing the power dissipation
   (c) reducing the chip size
   (d) all of these.

   (x) Stick Diagram represents
   (a) logic (b) circuit
   (c) layout (d) architecture.

Group – B

2. (a) Explain the modes of operation of MOS transistors in enhancement mode.

   (b) Compare the characteristics of NMOS vs CMOS inverters in terms of noise margin and power dissipation.

   8 + 4 = 12

3. (a) What is the difference between "Micron based Design Rule" and "Lambda Based Design Rule"?

   (b) What are differences between Full Custom Design and Standard Cell based Semi Custom Design?

   (c) Draw schematic of CMOS gate that represents following function f = (A + B + CD).

   (d) Draw Stick Diagram of the same CMOS gate.

   2 + 2 + 3 + 5 = 12

Group – C

4. (a) Draw Y Chart for VLSI Design.

   (b) Draw Flow Diagram of VLSI Design Cycle.

   (c) Draw Flow Diagram of Front End Design Flow.

   (d) Write Verilog behavioural model for a D – Flip Flop.

   3 + 3 + 3 + 3 =12

5. (a) Define Physical design.

   (b) Mention the need of physical design in VLSI.

   (c) Explain various steps of physical design.

   (d) What is Standard Cell design? How does it differ from gate-array design?

   3 + 3 + 3 + 3 = 12

Group – D

6. (a) Draw Flow Diagram of Physical Layout Automation

   (b) For the following Channel Routing Problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)
   Terminal Connection is as follows:
   11122563040 ----- Upper Boundary
   25055330604 ----- Lower Boundary
   0 means no Connection.
   Assume HV Layer (V = Metal 1, H = Metal 2)

   (c) Provide Optimum Channel Routing Solution for above case using Left Edge Algorithm.

2 + 5 + 5 = 12

7. (a) Draw flow diagram of High Level Synthesis.

   (b) Draw flow diagram of Logic Synthesis.

   (c) Draw BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using ordering of a $\leq$ b $\leq$ c.

   (d) Create ROBDD Diagram and corresponding optimized Boolean expression.

3 + 3 + 3 + 3 = 12

Group – E

8. (a) Write Verilog program of 2:1 MUX using Continuous assignment (Dataflow) style.

   (b) Write Verilog program for 3 to 8 decoder using always and case statements.

   (c) Write Verilog program of resettable UP counter.

4 + 4 + 4 = 12

9. Write short notes on following topics **(3 × 4) = 12**
   (i) FPGA
   (ii) Finite State Machine
   (iii) Technology Library Mapping for Logic Synthesis.