B.TECH / IT /5TH SEM/ INFO 3102/2017
COMPUTER ARCHITECTURE
(INFO 3102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Under which of the following categories, Array processors will come?
(a) SISD (b) MIMD (c) SIMD (d) MISD.

(ii) CISC has
(a) unified cache (b) I and D cache
(c) L1 cache (d) None of these.

(iii) The number of machine instructions to be executed in the program is called
(a) Cycle (b) Time period
(c) Instruction count (d) None of these.

(iv) The distance between the vector elements is known as
(a) Stride (b) Hamming distance
(c) Euclidean distance (d) None of these.

(v) A mesh is an example of
(a) Dynamic network (b) Static network
(c) Switch (d) Omega network.

(vi) Content of program counter register changes in.....
(a) Data Hazard (b) Structural Hazard
(c) Control Hazard (d) None of these.

(vii) When block size is equal to entire cache size, then hit ratio becomes
(a) 1 (b) 2 (c) 0 (d) 4.

(viii) What will be the speed-up for a 4 segment linear pipeline when the number of instructions n=64?
(a) 4.5 (b) 3.82 (c) 8.16 (d) 2.95.

(ix) Superscalar pipeline have CPI of
(a) 1 (b) greater than 1
(c) less than 1 (d) greater than 2.

(x) Dynamic pipeline allows
(a) multiple functions to evaluate
(b) only streamline connection
(c) to perform fixed function
(d) none of these.

Group - B

2. (a) Explain different types of data hazard with suitable example. Differentiate between static scheduling and dynamic scheduling in pipeline.

(b) What is Arithmetic pipeline? Show the steps, an arithmetic pipeline execute to add two numbers (A, B). A = 0.9354×10^4 and B = 0.7522×10^3.

(c) What is Internal Forwarding? Explain different types of Internal Forwarding.

(3 + 2) + (1 + 3) + (1 + 2) = 12

3.(a)

Instruction type	Instruction Mix	CPI
Arithmetic	30%	1
Data transfer	10%	2
Floating point	30%	2
Control transfer	30%	4

Consider a benchmark program having 100000 instructions. To execute the program, the instruction pipeline is equipped with 5 stages and operates at a frequency of 50MHz. Penalties due to branch instruction are ignored. Calculate the effective CPI, MIPS rate, Throughput and Speed-up of the pipeline.

3.(b)

	1	2	3	4	5	6	7
S1	X					X	
S2		X		X			
S3			X				X
S4				X	X		

From the above reservation table, find the following:

(i) What are the forbidden latencies and initial collision vector?

(ii) Draw the state transition diagram.

(iii) Determine the MAL, upper and lower bounds of MAL for this pipeline.

4 + (2 + 4 + 2)=12

Group - C

4. (a) What do you mean by cache mapping? With a block diagram explain in detail about direct mapping technique of cache memory.

(b) A cache is 4 – way set-associative mapped and can store 64KB of data. Capacity of each cache block is 32 byte. The address is 32 bit wide. What are the sizes of the different sub-fields in this address?

(2 + 5) + 5=12

5. (a) Explain the concept of virtual memory organization with suitable diagram. Also explain the address translation procedure using page table.

(b) Explain the working principle of translation look aside buffer (TLB).

(4 + 4) + 4 = 12

Group - D

6. (a) Discuss the working of VLIW processor in detail with suitable diagram.

(b) Explain Dynamic scheduling with scoreboarding in detail. State and discuss different types of vector instruction.

4 + (4 + 4) = 12

7. (a) Explain the architectures of Array processor with necessary diagrams.

(b) Differentiate between Super-pipelining and Superscalar pipeline architecture with suitable diagrams.

(c) Discuss Microprogrammed Control unit with necessary diagram and clearly state each component of the unit.

4 + 4 + 4= 12

Group - D

8. (a) Explain Snoopy cache coherence protocol in detail.

(b) Differentiate between Data flow architecture and Control flow architecture (Any Four).

(c) Explain Flynn's classification of parallel architectures in detail

4 + 4 + 4= 12

9.(a) Draw an 8 - input Omega network using 2 × 2 switches as building blocks. Show the switch settings for the following permutations.
(1, 3, 4, 7, 6) (3, 2) (5).

(b) Draw data flow graph to represent the following computations:

(i) A= P + Q

(ii) B=A / Q

(iii) C=P*A

(iv) D=C-B

(v) E=C*A

(vi) F=D/E

(4 + 4) + 4= 12