B.TECH / IT /3RD SEM/ INFO 2102/2017
COMPUTER ORGANIZATION
(INFO 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Thrashing
(a) reduces page I/O (b) reduces degree of multiprogramming.
(c) implies excessive page I/O (d)none if these.

(ii) A page fault
(a) occurs when a program access a page memory
(b) is an error in specific page
(c) is an access to a page not currently in memory
(d) none of these.

(iii) Instruction cycle is
(a) fetch-decode-execution (b) fetch-execution-decode
(c) decode-fetch-execution (d) fetch-decode-execution-store.

(iv) How many address lines are needed to address each memory location in 2046 × 4 memory chip?
(a) 8 (b) 10 (c) 11 (d)12.

(v) How many RAM chips of size(256k × 1 bit) are required to build 1MB memory?
(a) 8 (b) 16 (c) 32 (d)64.

(vi) Booth's algorithm of multiplication is used for
(a) multiplication of signed 2's complement number.
(b) multiplication of signed 1's complement number.
(c) division of any number
(d) none of the above.

(vii) Micro instructions are kept in
(a) control memory (b) cache memory
(c) main memory (d) secondary memory.

(viii) The cache memory bridges the speed gap between _____ and ____.
(a) RAM and ROM (b) RAM and Secondary memory
(c) main memory (d) secondary memory.

(ix) The value of biased exponent in IEEE754 single precision format is
(a) 127 (b) 254 (c) 128 (d)256.

(x) "Delayed Branching" is related to
(a) Pipeline Hazard (b) Pipe line remedy
(c) both a & b (d) none of these.

Group - B

2 . (a) Differentiate between computer organization and computer architecture. Explain relative advantages and disadvantages between Direct Addressing Mode and Indirect Addressing Mode with example.

(b) Draw and explain VON-Neumann Architecture.

(2 + 4) + 6 =12

3. (a) What are the different types of instruction formats? Explain briefly.

(b) Using ZERO address instruction evaluate the following arithmetic instruction:

X=(A-B+C*(D*E-F))/(G+H*K).

6 + 6 =12

Group - C

4. (a) Derive the working principle of Carry Look Ahead adder. What is the advantage of Carry Look Ahead Adder over Ripple Carry Adder?

(b) Multiply (-13) and (-9) with the help of any suitable multiplication algorithm.

(4 + 2) + 6 =12

5. (a) Represent $(1101011)_2$ in IEEE 754 double precision format. What is the use of biased exponent?

(b) Draw the flowchart of Restoring type of Division algorithm. Divide 15 by 3 with the help restoring type of division method.

(4 + 2) + (3 + 3) =12

Group – D

6. (a) Write the differences between SRAM and DRAM?.

(b) Write the expression to calculate average access time for 2-level cache memory and clearly state each term of the expression.

(c) Let a computer system has cache capacity 64 KB, Main Memory capacity 1 MB, 2 KB page size, pages per set are 2. Show the size & different address fields in direct and set-associative mapping.

2 + 2 + (4 + 4) = 12

7. (a) What are the differences between virtual memory and primary memory? How virtual memory address is converted to physical address? Explain with an example.

(b) For a computer system the page references are 7 0 1 2 0 3 0 4 2 3 0 3 2 having four frames. Calculate Hit and Miss ratio using FCFS and LRU page replacement algorithm.

(2 + 4) + (3 + 3) = 12

Group – E

8. (a) Derive the expression of speed-up calculation of a pipelined architecture. Then prove that the speed-up $S \alpha K$, where K is the no of pipelines stages. Also calculate the efficiency and throughput of the architecture.

(b) What is Pipeline Hazard? Describe different types of Hazard present in Pipeline based system.

(3 +1 + 1 +1) + (2+4) = 12

9. (a) What is interrupt? What are the differences between vectored and non vectored interrupt?

(b) Explain the concept of DMA transfer with evitable diagram.

(2 + 4) + (3 + 3) = 12