B.TECH / IT /3RD SEM/ INFO 2101/2017
DIGITAL ELECTRONICS
(INFO 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The number of FFs required in a mod - 8 counter is _____.
(a) 3 (b) 4 (c) 5 (d) 6.

(ii) How many flip – flops are needed to divide the input frequency by 64?
(a) 2 (b) 4 (c) 6 (d) 8.

(iii) A MUX with its address bits generated by a counter operates as a :
(a) Parallel to Serial converter (b) Serial to Parallel converter
(c) Modified counter (d) Modified MUX.

(iv) The minimum number of 2 input NAND gate required to realize Full Adder circuit is:
(a) 6 (b) 7 (c) 8 (d) 9.

(v) The NAND-NAND realization is equivalent to :
(a) AND-NOT (b) OR-NOT
(c) AND-OR (d) NOT-OR.

(vi) How many select lines are required for a 1024:1 MUX?
(a) 65 (b) 10 (c) 128 (d) 256.

(vii) The code used for labelling the cells of k-map is :
(a) Gray code (b) Octal code
(c) BCD (d) Hexadecimal .

(viii) The most expensive ADC is:
(a) Dual Slope Type (b) Ramp Type
(c) Successive Approximation Type
(d) Flash ADC .

(ix) Which of the following logic family has highest noise margin?
(a) TTL (b) CMOS (c) RTL (d) ECL.

(x) Let f(A, B) = A' + B. Simplified expression for function f(f(x + y, y), z) is :
(a) x' + z (b) xyz (c) xy' + z (d) x.

Group - B

2.(a) Draw a logic circuit to convert binary code $y_1\ y_2\ y_3$ to gray code.

(b) Derive a logic expression that will be equal to 1 only when two binary number A_1A_0 and B_1B_0 have same values. Draw circuit diagram and construct truth table to verify this logic.

(c) Identify the Essential Prime Implicants (EPI) in k-map for the following function :
$F(A, B, C, D) = \sum m(0, 4, 5, 10, 11, 13, 15)$.

3 + 6 + 3 =12

3. (a) Minimize the following expression using Boolean algebra:
i) f= AB' C+ B + BD' + ABD' + A'C
ii) f= AB[AC + (B + C')D].

(b) What are don't care combinations? Minimize the following switching function to the simplest possible POS forms:
$F(A, B, C, D) = \sum m(1,4,7,10,13) + \sum d(5,14,15)$.
where d denotes don't care condition.

4+ (2 + 6) = 12

Group - C

4. (a) Design a SR flip-flop using D flip-flops.

(b) Implement the following logic function using 8 × 1 MUX considering D as the input and A, B, C as the selection lines: F(A, B, C, D)=AB' + BD + B' CD.

5 + 7= 12

5. (a) Design a combinational circuit which will accept a 3-bit binary number and will generate an output binary number equal to the square of input number.

(b) Design a BCD to Gray code converter.

6 + 6 = 12

Group – D

6. (a) Design a MOD – 10 counter.

(b) Design a 4 – bit Parallel – in Serial – out (PISO) register.

8 +4 =12

7. Design a sequence detector that produces an output 1 whenever the sequence 10101 is detected.

12

Group – E

8. (a) Explain the operation principle of Successive Approximation type ADC with suitable diagram.

   (b) The logic levels used in a 4 bit R-2R ladder DAC are : 1 = 5V and 0 = 0V. Find the output voltage for input 0010.

6 + 6= 12

9. (a) Mention and compare the different logic families. Why is a dual slope ADC preferred in a digital voltmeter.

   (b) A 5 bit DAC produces an output of 0.1 V for a digital input of 00001. What is the full scale output? Find the output for an input of 10101.

(2 + 4 + 2)+ 4 =12