B.TECH/ECE/6TH SEM/ECEN 3201/2017

DIGITAL VLSI DESIGN
(ECEN 3201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Why is substrate of NMOS connected to ground in a CMOS inverter?
(a) To forward bias the drain with respect to substrate
(b) To forward bias the source with respect to substrate
(c) To stop current flow through the substrate
(d) To create the channel between drain and source.

(ii) Which of the following CMOS logic circuit will contain parallel NMOS transistors?
(a) NOR (b) NAND
(c) Transmission gate (d) Inverter.

(iii) BDD is used in
(a) High Level Synthesis (b) Logic Synthesis
(c) Floorplan (d) Routing.

(iv) Minimum number of transistors in CMOS logic Y = AB + CD + EF is
(a) 10 (b) 12 (c) 14 (d) 8.

(v) Which of the following is a process of transforming design entry information of the circuit into a set of logic equations?
(a) Simulation (b) Optimization
(c) Synthesis (d) Verification.

(vi) KL Algorithm is related to
(a) Routing (b) Partitioning
(c) Logic Synthesis (d) High Level Synthesis.

(vii) Which of the following is the main architecture block of a PLD?
(a) Logic cell (b) Memory
(c) Microprocessor (d) Switch.

(viii) In layout designing, minimum Feature Size represents
(a) the distance between Source and Drain, set by minimum width of polysilicon
(b) the distance between Source and Gate, set by minimum width of polysilicon
(c) the distance between Gate and Drain, set by minimum width of polysilicon
(d) width of inter-connect.

(ix) In which of the following VLSI methodology most manual effort is needed?
(a) FPGA (b) Gate Array
(c) Std Cell Based Semi Custom (d) Full Custom.

(x) 0.7 Technology Scaling enables layout area scaling of
(a) 0.7 (b) 0.5 (c) 0.45 (d) 0.65.

Group – B

2. (a) Design a CMOS gate for the logic function $f(x_1, x_2, x_3) = \Sigma m(0, 1, 2, 6, 7)$. Mention the widths of the NMOS and PMOS for the above design so that the current driving capability remains same as that of the basic CMOS inverter.

   (b) Draw the VTC curve of a CMOS inverter and mention the regions of operation of both NMOS and PMOS at various input conditions.

(6 + 2) + 4 = 12

3. (a) What are differences between Full Custom Design and Std Cell based Semi Custom Design?

   (b) Draw Circuit Diagram of 2 input XOR gate using CMOS Logic.

   (c) Draw Circuit Diagram of 2 input XOR gate using CMOS Transmission Gate (TG).

4 + 4 + 4 = 12

Group – C

4. (a) Design a positive edge-triggered Master-Slave D-flipflop using Transmission Gate logic and draw the output waveform.

   (b) Design a static CMOS circuit of the function Y = (AB + CD + E)' and construct its layout using Euler Path Algorithm.

5 + 7 = 12

5. (a) Draw Layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

   (b) What is the difference between "Micron based Design Rule" and "Lambda Based Design Rule"?

   (c) Draw schematic and Stick Diagram of 2 input NOR gate.

4 + 3 + 5 = 12

Group – D

6. (a) Write Verilog Description of a D-Flipflop.

   (b) Write Verilog Description of a 3 to 8 Decoder.

   (c) Write Verilog Description of a 0, 1, 2, 4, 9, 10, 5, 6, 8, 7, 0 .... Sequence Counter.

4 + 4 + 4 = 12

7. (a) What do you mean by Bit Swizzling? State with example the types of circuit modelling using HDL.

   (b) Write an HDL module for a 2 : 4 decoder.

   (c) Discuss the limitations of RTL synthesis.

6 + 4 + 2 = 12

Group – E

8. (a) Explain the different kinds of physical faults that can occur on a CMOS chip and relate them to typical circuit failures.

   (b) Explain D-Algorithm.

7 + 5 = 12

9. (a) Draw Circuit diagram of Scan Flip Flop and explain how it works.

   (b) Draw block diagram of Scan Design/Structure and explain its operation.

6 + 6 = 12