(vi)

1) Virtual Memory	i) Conflicts
2) Cache Memory	ii) Pages
3) Cache Coherence	iii) Blocks
4) Direct Mapped Cache	iv) Multiprocessor Caches

Which of the following gives the correct matching?
(a) 1-i, 2-ii, 3-iii, 4-iv (b) 1-ii, 2-iii, 3-iv, 4-i
(c) 1-ii, 2-iii, 3-i, 4-iv (d) none of the above.

(vii) Superscalar processors have CPI of
(a) less than 1 (b) greater than 1
(c) more than 2 (d) greater than 3.

(viii) Dynamic pipeline allows
(a) multiples function to evaluate
(b) only streamline connection
(c) to perform fixed function
(d) none of these.

(ix) Assume a 8-stage instruction pipeline. The probability of a branch instruction in an instruction stream is 0.2. There is a 50% chance of a branch being taken. What is the degradation in pipeline performance?
(a) 40% (b) 41% (c) 45% (d) 46%.

(x) Stride in vector processor is used to
(a) differentiate different data types
(b) differentiate different registers
(c) differentiate different data
(d) none of the above.

Group - B

2. Consider the following reservation table. Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the pipeline. Find out simple cycle, greedy cycle and MAL. What are the bounds on MAL?

	1	2	3	4
S1	X			X
S2		X		
S3			X	

2 + 4 + 4 + 2 = 12

(c) Suppose you have n^r processors at your disposal. You ha algorithm like the Matrix multiplication which has $O(n^3)$ complexity. You know using O(n) number of parallel proc elements you can design an algorithm which will run in $O(n^2)$ Also an algorithm exists with O(n) complexity using $O(n^2)$ num processing elements. Does this mean you can you get complexities $O(n^{3-r})$ for r > 3? What interesting event would occurred had this been achievable?

5 + 4 + 3

Group - E

8. (a) Suppose that in an MIMD system, there are 10 processors. Eac its own cache. Suppose two processors each caches a single s variable X. How many messages are sent across the syste maintaining cache coherency of X if a) Snooping protocol is us If a Centralized Directory Based Protocol is used? Explain answer.

(b) For the following instruction sequence draw the correspondin Flow Graph:

1. P = X + Y
2. Q = P ÷ Y
3. R = X × P
4. S = R − Q
5. T = R × P
6. U = S ÷ T

(c) Suppose you gave an example of a WAR hazard as follows:
I1: ADD R1,R2; R2 <- (R1) + (R2)
I2: MOV A, R1; R1 <- [A];

Note here that R1 is a likely candidate for WAR hazard. Ca explain what would be a necessary condition for this WAR haz occur? Now you claim that just by modifying R1 to R3 in I2 solv problem. Is this always correct? Please explain briefly.

4 + 4 + (2 + 2

9. (a) Which of the following design options are chosen for a RISC architecture and why?

(i) Fixed vs. variable length instruction format
(ii) Simple vs. complex addressing mode
(iii) Load-store architecture

(b) Explain the fundamental difference in interprocessor communication mechanism between a multiprocessor and a multicomputer system.

(c) Point out the essential differences between Control Flow and Data Flow machines.

6 + 3 + 3 = 12

2016

COMPUTER ARCHITECTURE
(CSEN 2203)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: **10 × 1 = 10**

(i) The performance of a pipelined processor suffers if
(a) the pipeline stages have different delays
(b) consecutive instructions are dependent on each other
(c) the pipeline stages share hardware resources
(d) all of these.

(ii) The number of cycles required to complete n tasks with k stage pipeline is
(a) k+n-1 (b) k (c) nk+1 (d) none of these.

(iii) There is a pipeline with 4 stages. The number of instructions is 40. What will be the approximate speed-up of this circuit?
(a) 1 (b) 2 (c) 3 (d) 4.

(iv) The prefetching is a solution for
(a) data hazard (b) structural hazard
(c) control hazard (d) none of these.

(v) A 64 input Omega Network requires how many stages of 2 × 2 switches?
(a) 6 (b) 64 (c) 8 (d) 4.

3. (a) WAR and WAW hazards cannot occur in plain vanilla pipeline - why? What is a very necessary precondition for occurrence of these types of hazards?

(b) Explain what is meant by a Static and a Dynamic pipeline. Can you have a static pipeline which is multifunctional? Can you have a dynamic pipeline which implements a single function only? Explain briefly.

(c) How can hazard occur in executing the following set of instructions?

I1: MOV R1,A; [A] <- (R1)
I2: ADD R2,R3; R3 <- (R3) + (R2)
I3: SUB R4,R5; R5 <- (R4) – (R5)
I4: NOP

All the symbols have their usual meanings. You may assume a pipeline unit consisting of four stages.

(d) "Instruction execution throughput increases in proportion with the number of pipeline stages". Is it true? Justify your statement.

3 + 3 + 3 + 3 = 12

Group - C

4. (a) Explain Multistage implementation of a Cube Network with a suitable diagram.

(b) Consider the following program: (assume Opcode <srec>,<dest> format):

Add R3, R2
Sub R3,R4
Add R2,R1
Mov R1,[R4] ; writes to memory location
;pointed to by R4
Jnz R1, ThisPlace
: : : : : :
ThisPlace: <some code>

Assuming a delay slot value of 3, rewrite the code to exploit the Delayed Branching mechanism. Explain briefly how performance is improved because of application of the above technique.

(c) Explain why Memory-to-Memory architecture is not possible in a Array or Vector Processor Architecture.

4 + 5 + 3 = 12

B.TECH/CSE/4TH SEM /CSEN 2203/2016

3. (a) WAR and WAW hazards cannot occur in plain vanilla pipeline - why? What is a very necessary precondition for occurrence of these types of hazards?

(b) Explain what is meant by a Static and a Dynamic pipeline. Can you have a static pipeline which is multifunctional? Can you have a dynamic pipeline which implements a single function only? Explain briefly.

(c) How can hazard occur in executing the following set of instructions?

I1: MOV R1,A; [A] <- (R1)
I2: ADD R2,R3; R3 <- (R3) + (R2)
I3: SUB R4,R5; R5 <- (R4) – (R5)
I4: NOP

All the symbols have their usual meanings. You may assume a pipeline unit consisting of four stages.

(d) "Instruction execution throughput increases in proportion with the number of pipeline stages". Is it true? Justify your statement.

3 + 3 + 3 + 3 = 12

Group - C

4. (a) Explain Multistage implementation of a Cube Network with a suitable diagram.

(b) Consider the following program: (assume Opcode <srec>,<dest> format):

Add R3, R2
Sub R3,R4
Add R2,R1
Mov R1,[R4] ; writes to memory location
;pointed to by R4
Jnz R1, ThisPlace
: : : : : :
ThisPlace: <some code>

Assuming a delay slot value of 3, rewrite the code to exploit the Delayed Branching mechanism. Explain briefly how performance is improved because of application of the above technique.

(c) Explain why Memory-to-Memory architecture is not possible in a Array or Vector Processor Architecture.

4 + 5 + 3 = 12

CSEN 2203 3

5. (a) What do you mean by the perfect shuffle operation? How is the Omega NW configured to implement the perfect shuffle operation?

(b) Implement data routing logic of SIMD architecture to compute

$$s(k) = \sum_{i=0}^{k} At \text{ for } k = 0, 1, 2 \ldots N-1.$$

(c) Why do we need masking mechanism in SIMD array processors?

(2+2) + 5 + 3 =12

Group - D

6. (a) With simple diagram explain data flow architecture. Compare with Control Flow architecture.

(b) Draw data flow graph for the following set of instructions:

X = A+B
Y=X/B
Z=A*X
M=Z–Y
N=Z*X
P=M/N

(c) Explain register to register architecture.

5 +4 + 3 = 12

7. (a) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts :

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	50000	2
Data Transfer	70000	3
Floating point arithmetic	25000	1
Branch	4000	2

Calculate the effective CPI, MIPS rate and execution time for this program

(b) Using multiple functional pipeline units you can avoid structural hazards - explain briefly. How is this concept used very effectively in constructing superscalar processors?

B.TECH/CSE/4TH SEM /CSEN 2203/2016

5. (a) What do you mean by the perfect shuffle operation? How Omega NW configured to implement the perfect shuffle operati

(b) Implement data routing logic of SIMD architecture to compute

$$s(k) = \sum_{i=0}^{k} At \text{ for } k = 0, 1, 2 \ldots N-1.$$

(c) Why do we need masking mechanism in SIMD array processors

(2+2) + 5 +

Group - D

6. (a) With simple diagram explain data flow architecture. Compare v Control Flow architecture.

(b) Draw data flow graph for the following set of instructions:

X = A+B
Y=X/B
Z=A*X
M=Z–Y
N=Z*X
P=M/N

(c) Explain register to register architecture.

5 +4 + 3

7. (a) A 50 MHz processor was used to execute a program wit following instruction mix and clock cycle counts :

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	50000	2
Data Transfer	70000	3
Floating point arithmetic	25000	1
Branch	4000	2

Calculate the effective CPI, MIPS rate and execution time fo program

(b) Using multiple functional pipeline units you can avoid stru hazards - explain briefly. How is this concept used very effectiv constructing superscalar processors?