B.TECH/CSE/5TH SEM/AEIE 3105/2016

MICROPROCESSORS & MICROCONTROLLERS
(AEIE 3105)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) If A_0, A_1 pins of 8255 are 00, which port is selected
(a) port A (b) port B (c) port C (d) none of these.

(ii) 8259 is a
(a) programmable interrupt controller
(b) DMA controller
(c) programmable keyboard display controller
(d) programmable counter.

(iii) Which of the following is invalid instruction?
(a) STAX H (b) XCHG (c) ADC M (d) LHLD 1234H.

(iv) Among the following which one have 20 address lines?
(a) 8251 (b) 8051 (c) 8086 (d) 8255.

(v) In 8086 how many flag bits are there in flag register?
(a) 16 (b) 9 (c) 5 (d) 8.

(vi) In order to enable TRAP, which of the following instruction are needed?
(a) EI (b) SIM (c) EI & SIM (d) None of these.

(vii) In 8085, RST 1 is –
(a) Ending Instruction (b) Vectored Interrupt
(c) S/w Interrupt (d) None of the above.

(viii) Instruction register holds
(a) flag condition (b) opcode
(c) instruction address (d) hex code.

(ix) What is the BSR control word to set PC_4?
(a) 09_H (b) 07_H (c) 04_H (d) 05_H.

(x) The number of T-States required for MOV B, M is
(a) 4 (b) 7 (c) 10 (d) none of them.

Group – B

2. (a) What are the functions of ALE, HOLD, $\overline{INTA}$ of 8085 microprocessor?

(b) Calculate the time delay for the following loop in 8085 microprocessor.
Assuming that the frequency = 2MHZ.

```
    LXI D 238H
L1: DCX B
    MOV A, C
    ORA D
    JNZ L1
```

6 + 6 = 12

3. (a) How many hardware interrupts are there in 8085? Explain with block diagram.

(b) Draw the timing diagram of MVI M, $9E_H$.

6 + 6 = 12

Group – C

4. (a) Draw the timing diagram for Opcode-fetch cycle.

(b) An 8k × 8 RAM is interfaced with 8085A using a NAND gate decoder. Now calculate the final address of the chip if initial accessible address is 4000H.

(c) Write down a program to generate first 10 values in a Fibonacci Series.

4 + 2 + 6 = 12

5. (a) What are the main feature performed by BIU, EU units of 8086 microprocessor?

(b) How is pipeline achieved in 8086 microprocessor? Describe the min and max mode signal of 8086 microprocessor.

4 + (4 + 4) = 12

Group – D

6. (a) Discuss on memory organization of 8051 microcontroller.

   (b) What area the different available addressing modes in case of 8051.

   (c) Explain the timer with mode 0 and mode 1.

4 + 4 + 4 = 12

7. (a) Differentiate between RISC and CISC architecture. Which of the these architecture is followed in PIC microcontroller? How many instructions are there in the instruction set of PIC 16F84?

   (b) Describe the bit significance of TMOD register in 8051 Microcontroller.

   (c) Describe the significance of following pins of 8051 Microcontroller *(Any two)*:
   XTAL1-XTAL2, P0.0-P0.7, $\overline{EA}$ / VPP,

(2 + 1 + 1) + 4 + 4 = 12

Group – E

8. (a) Describe the purpose of various bits of port-C of an 8255A when port A and port B both are set as i/p port in mode 1.

   (b) Describe the control word bit significance for BSR mode.

   (c) Write short notes on DMAc 8237A.

6 + 2 + 4 = 12

9. (a) Interface two 3k*8 RAM with 8085 microprocessor by using IC 74138 decoder such that the starting address to them are 8000H and 9000H respectively.
   Calculate the memory chip needed to design 8kb memory if the memory size is of 1024*1 bit.

   (b) Difference between memory mapped I/O, and peripheral mapped I/O.

(6 + 2) + 4 = 12