# B.Tech/CSE/3rd Sem/ECEN-2104/2015

## 2015

## DIGITAL LOGIC AND COMPUTER ORGANIZATION

## (ECEN 2104)

*Time Alloted : 3 Hours* *Full Marks : 70*

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable***

### GROUP - A

**(Multiple Choice Type Questions)**

1. Choose the correct alternatives for the following : **[10×1=10]**

   i) Micro instructions are kept in

   (a) Main Memory (b) Control Memory
   (c) Cache Memory (d) Secondary Memory

   ii) Principle of locality justifies the use of

   (a) DMA (b) Paging
   (c) Cache Memory (d) Polling

   iii) If (24 + 17) = 40 then the base of the numbers is

   (a) 5 (b) 6
   (c) 9 (d) 11





   iv) In which addressing mode the effective address of the operand is generated by adding a constant value to the contents of the register?

   (a) Indexed (b) Indirect
   (c) Register (d) Absolute

   v) The capacity of a memory unit is defined by the number of words multiplied by the number of bits per word. How many separate address and data lines are needed for a memory 4K × 16?

   (a) 10 addresses, 16 data lines
   (b) 11 addresses, 8 data lines
   (c) 12 addresses, 16 data lines
   (d) 12 addresses, 12 data lines

   vi) A carry look ahead adder frequently used

   (a) is faster (b) is more accurate
   (c) uses fewer gates (d) costs less

   vii) Two 4-bit 2's complements of binary numbers 1011 and 0110 are added. Then the result will be

   (a) 1111 (b) 0010
   (c) 1101 (d) 0001

   viii) Minimum number of NAND gates required to implement the X-OR gate for two variables is

   (a) 5 (b) 7
   (c) 4 (d) 3

   ix) A 3 bit MOD-8 ripple counter uses JK flip-flops. If the propagation delay of each flip-flop is 50 nS then the minimum input clock frequency will be

   (a) 5 MHz (b) 6.6 MHz
   (c) 8.67 MHz (d) None of these

x) The dual of the Boolean theorem A(B + C) = AB is

(a) A + BC = (A + B)(A + C)

(b) ABC = (A + B)(A + C)

(c) AB + AC = (A + B)(A + C)

(d) None of these

## GROUP - B

2. (a) (i) Add - 89.75 to + 43.25 using 12 bit 1's complement method.

(ii) Subtract 14 from 46 using 8 bit 2's complement method.

(b) Prove that : $A\left[B+\overline{C}\left(\overline{AB+A\overline{C}}\right)\right]=AB$

(c) Draw a BCD adder circuit to add two BCD numbers. The output of this adder circuit should be in BCD.

**(2+2)+3+5 = 12**

3. (a) For the function $f(w,x,y,z)=\Sigma(0,1,2,3,4,6,7,8,9,11,15)$ find out all prime implicants and indicate which are essential.

(b) Implement a full adder and a full subtractor circuit using a 3-to-8 decoder.

(c) What is the limitation of K-Map?

**6+5+1 = 12**

## GROUP - C

4. (a) Design a Full Adder and Subtractor module using two Half Adders and appropriate gates.

(b) Design a J K Master slave flip flop using two clocked R S Flip flop.





(c) Design the following function using appropriate Multiplexer F(A,B,C) = S(1,3,5,7)

**4+4+4 = 12**

5. (a) Evaluate the following expression in a zero address and one address machine

Y = (A - B) / (C + D*E)

(b) Show how a 4-bit Carry look ahead adder performs faster than an 4-bit ripple carry adder.

(c) Defferentiate between compiler and assembler. Mention the advantage of floating point representation of numbers.

**4+4+4 = 12**

## Group - D

6. (a) Distinguish between SRAM and DRAM. Explain their reading and writing operation.

(b) What is cache mapping? Explain direct mapping for 256 × 8 Ram and 64 × 8 Cache memory. Briefly explain the functionality of an associative memory.

**6+(2+2+2) = 12**

7. (a) What is a virtual memory? Why is it called virtual? What are the advantages of a virtual memory?

(b) What is a page? What is demand paging? What is a page fault?.

(c) What are the various page replacement policies?

**(2+1+1)+(2+2+1)+3 = 12**

## GROUP - E

8. (a) Compare the pros and cons of RISC and CISC based architecture.

(b) What are the differences between a hardwired control unit and a micro-programmed control unit?

(c) The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two word call subroutine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP, and the top of the stack

(i) before the call instruction is fetched from memory?

(ii) after the call instruction is executed?

(iii) after the return from subroutline?

**5+4+3 = 12**

9. (a) Why is DMA based I/O better than other I/O technique?

(b) Differentiate between isolated I/O and memory mapped I/O?

(c) Explain DMA data transfer between memory and terminal peripheral.

(d) Differentiate between vectored and non vectored interrupt?

**3+3+4+2 = 12**