COMPUTER ORGANIZATION AND ARCHITECTURE
(MCAP 1205)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The principle of locality of reference justifies the use of
(a) cache memory (b) interrupt
(c) polling (d) DMA.

(ii) Instruction cycle is
(a) fetch-decode-execution (b) fetch-execution-decode
(c) decode-fetch-execution (d) none of these.

(iii) Floating point representation is used to store
(a) boolean values (b) whole numbers
(c) real integers (d) integers.

(iv) The average time required to reach a storage location in memory and obtain its contents is called the
(a) seek time (b) turnaround time
(c) access time (d) transfer time.

(v) With 2's complement representation the range of values that can be represented on the data bus of an 8 bit microprocessor is given by
(a) -128 to +127 (b) -128 to +128
(c) -127 to +128 (d) 0 to 255.

(vi) The addressing mode used in an instruction of the form ADD X Y, is
(a) absolute (b) indirect (c) index (d) immediate.

(vii) In a program using subroutine call instruction, it is necessary to
(a) initialise program counter (b) clear the accumulator
(c) reset the microprocessor (d) clear the instruction register.

(viii) In a microprocessor the address of the next executable instruction is stored in the
(a) SP (b) PC (c) IR (d) none of these.

(ix) Pipeline implements
(a) fetch instruction (b) decode instruction
(c) fetch operand (d) calculate operand.

(x) Associative memory is
(a) a very cheap memory
(b) pointer addressable memory
(c) content addressable memory
(d) all of these.

Group – B

2. (a) Explain the importance of different addressing modes in computer architecture with suitable example.

(b) What is the difference between RISC & CISC?

(c) What is the difference between software interrupt and a subroutine call?

5 + 4 + 3 = 12

3. (a) "It is advantageous of using interrupt initiated data transfer over transfer under program control without an interrupt" – justify.

(b) Explain instruction cycle and interrupt cycle with example. Draw the flow-chart for instruction cycle.

5 + (4 + 3) = 12

Group – C

4. (a) Design the hardware of addition & subtraction of fixed point signed magnitude numbers.

(b) Briefly explain the storage layout for IEEE standard 754 floating point numbers for single precision and double precision numbers. Represent $(13.625)_{10}$ in IEEE 754 standard full-precision format as single precision number.

6 + (4 + 2) = 12

5. (a) Apply booth's algorithm to multiply the two numbers (-9) and (6). Assume multiplicand and multiplier to be 5 bits each.

(b) With the help of flow chart, discuss the hardware division algorithm. Explain how the divide overflow conditions are handled. Differentiate restoring and non restoring division.

5 + (2 + 3 + 2) = 12

Group – D

6. (a) What is cache coherency and how is it eliminated?

(b) What is write-back and write-through protocol? What are different types of DMA controllers and how do they differ in their functioning?

5 + (2 + 2 + 3) = 12

7. (a) What are hit rate and miss penalty?

(b) Draw a memory hierarchy with respect to size, speed and cost per bit.

(c) Compare the functionalities of direct mapping, associative mapping and set-associative mapping with their advantages and disadvantages.

3 + 3 + 6 = 12

Group – E

8. (a) Explain vector processing. What is the difference between vector & array processing?

(b) What is the difference between isolated I/O and memory mapped I/O?

(3 + 4) + 5 = 12

9. (a) What is speedup, throughput and efficiency of a pipelined architecture?

(b) Explain the hazards to the instruction pipeline with their solution.

(2 + 2 + 2) + 6 = 12